Research frontiers in DFT and BIST

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Introduction

- Evolution of DFT techniques for random logic and memory
  - Scan-path test access: adoption started ~1986; widely used now
  - Boundary scan: adoption started ~1993; widely used
  - Memory BIST: adoption started ~1996; widely used
    - At-speed → programmable → memory write-through
  - Scan compression: adoption started ~2001; increasing usage
    - 10X~100X compression → at-speed → controlled power
  - Logic BIST: adoption started ~2003; increasing usage
    - At-speed → async. multi-frequency → controlled power

- Evolution of DFT techniques for analog/mixed-signal/RF
  - Loopback, and analog bus – adoption started ~1975; widely used
  - BIST – ad hoc; minimal adoption

- System-on-chip test effort and costs: 70% mixed-signal
  - As reported by Infineon, Qualcomm (for cellphone ICs)
  - Need systematic DFT!
Outline

- 3D test problems, and DFT standards
  - Some details for 1149.4 and P1687
- Review of industry techniques for mixed-signal DFT/BIST
  - PLL
  - SerDes
  - DDR I/Os
  - Other I/Os
  - ADC/DAC
  - Analog
  - RF
- Conclusions
3D test problems

- Require known good die (KGD)
  - Final-test fault coverage at wafer-sort
  - Inductance+resistance of probe access

- Reduced access after packaging
  - Fewer pins per IC than single die packages
  - No visual access to each die for diagnosis

- More chip I/Os (TSVs)
  - Reduced area per I/O for test circuitry
  - Higher probability of faulty connections to other ICs

- Higher defectivity at package-level
  - Many ICs per package (with lower pre-package fault coverage)
  - TSV yield needs improvement
DFT standards for 3D applications

- Must test packaged IC via only 1149.x interface

- IEEE standards for testing chip I/Os and connections
  - 1149.1 (JTAG boundary scan) – 4 or 5 pins
    - Detect shorts/opens between connected I/Os, and control BIST
  - 1149.4 (analog boundary scan) – additional 2 or 4 pins
    - Apply currents and measure voltages at I/Os, and in core
  - 1149.6 (ACJTAG) – boundary scan for differential or AC interconnect
    - Apply TCK-rate square waves, and detect edge pulses
  - 1149.7 – reduced-pin 1149.1 test access ports
    - Also allows multiple TAPs to share same package pins

- IEEE standards for testing chip core
  - 1500 (embedded core test access) – scan wrappers & description
  - P1687 (IJTAG: Instrument JTAG) – access to test-instruments
  - P1838 (test access to 3D stacked ICs)

- Lots for digital; very little for analog
1149.4 standard mixed-signal (analog) test bus

- Overview presented to CMC May 16 by Heiko Ehrenberg
- IEEE issued in 2000, but updated in 2011 to include ABSDL
  - Analog boundary scan description language
  - Facilitates automated test generation
- Limitations, 4 solutions, more limitations
  - Maximum number of access-transistor diffusions per wire
    - DC leakage current before 100µA max reached \( \rightarrow \) <10 nodes is OK
    - AC coupling for HF signals, even in function mode \( \rightarrow \) good T switches
    - Capacitance limits bandwidth \( \rightarrow \) analog buffers
  - Maximum length of interconnect
    - Capacitance limits bandwidth; inductance limits SNR
    - Antenna effect/plasma-induced damage requires diffusions, capacitance
  - Solution: Multiple busses + analog multiplexer to AT1/AT2
    - Limitation: Wiring congestion if >200 nodes
    - Limitation: Still must traverse the whole IC
    - Limitation: Bus+switches+buffers limit bandwidth, SNR, linearity, offset
P1687 standard for on-chip instrument access

- Proposed IEEE standard
  - Being developed by >20 major companies
  - Standard digital access to on-chip test capabilities (instruments)

- Programmable length scan path access
  - Minimizes access time to any instrument

- Language that describes how to access any instrument
  - Allows automated retargeting of test patterns
  - Simplifies creation of test patterns
  - Facilitates creating tests that involve instruments on multiple ICs

Source: [http://grouper.ieee.org/groups/1687/documentation.html](http://grouper.ieee.org/groups/1687/documentation.html)
Analog/ mixed-signal DFT

- All DFT standards focus on digital
  - Except 1149.4, which hardly anyone uses
  - AMS test is growing to >70% of total test

- Overview of industry techniques for mixed-signal DFT
  - Focus on relevance to 3D
  - PLL
  - SerDes
  - DDR I/Os
  - General I/Os
  - ADC/DAC
  - Analog
  - RF

Key specifications
- DFT techniques
- BIST techniques
- Most common technique
- Emerging problems

Pie chart source: F. Poehl et al., “Production test challenges for highly integrated mobile phone SoCs - A case study”, Eur. Test Symp. 2010
PLL

- **Key specifications**
  - Jitter <5 ps rms
  - Duty cycle = 50% ±2%
  - Lock time <10 µs
  - Lock range = 100 MHz ~ 2 GHz

- **DFT techniques**
  - Connect divided-down clock to I/O pin to measure frequency, jitter
  - Connect analog bus to VCO control voltage to measure VCO range

- **BIST techniques**
  - Delay-line from ref. clock to sampling latch to measure jitter
  - Undersample with offset frequency to measure jitter, duty cycle
  - Count ref. clock cycles from forced loss-of-lock until lock regained

- **Most common technique**
  - No dedicated PLL test: simply wait lock time, then test core logic

- **Emerging problems**
  - All-digital PLLs – need prod’n test until proven in volume
  - PLL affects product-level specifications
Mentor’s Tessent PLLTest™

- Measures with calibrated 0.5ps~0.5ms resolution, in 10ms
- Jitter
  - Input, output
  - HF, LF
- Phase error
- Frequency, duty cycle
- Lock time, range
- Proven on customer silicon to <1 ps rms
- Sampling clock from another on-chip PLL, or off-chip PLL

US patent: 7158899
R. King & al., "Experiences with parametric BIST for production testing PLLs with picosecond precision", Int'T Test Conf., Nov. 2010

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SerDes I/O

**Key specifications (>4Gb/s)**
- Random jitter <2 ps rms
- Duty cycle = 50% ±1%
- Amplitude >500 mV
- ISI <20 ps p-p

**DFT techniques**
- In receiver, add 2nd comparator with adjust. V_{REF} to monitor signals
- Add multiple on-chip loopback paths (serial, parallel, pre/post filter)

**BIST techniques**
- PRBS generate+compare, for loopback bit error rate test (BERT)
- Programmable phase-interpolator to sample anywhere in signal eye
- Offset ref. frequency for receiver to undersample input signal

**Most common technique**
- Loopback PRBS, and detect no bit errors in <500 ms

**Emerging problems**
- ISI from inter-chip wiring dominates – must test equalization
- ATE too expensive, impractical >5 Gb/s
Mentor’s Tessent SerdesTest™

- Measures with calibrated 0.1ps~0.1ms resolution, in 10ms
- Waveform
  - Rise time, slew rate
- Jitter
  - $RJ_{RMS}$, $TJ_{RMS}$ (with LF rejection)
  - $DJ_{p-p}$ (DCD, ISI)
- Jitter tolerance
  - Equalization
  - Sampling instant (mean, variation)
  - BER
- Proven on customer silicon >10 Gb/s, >50 lanes, <1 ps rms
DDR I/O

- **Key specifications** (>800 Mb/s per pin)
  - Crosstalk <50 ps
  - Duty cycle = 50% ±1%
  - Slew rate ≈ 1V/ns
  - Skew <20 ps across 8 pins

- **DFT techniques**
  - Selectable DLL outputs to sample multiple time points in DQ signal

- **BIST techniques**
  - Pseudo-random word or 1010 generate+compare, for loopback
  - Delay line in clock for DQ pin receivers
  - Offset ref. frequency for receiver or boundary scan to undersample

- **Most common technique**
  - Functional testing by ATE

- **Emerging problems**
  - ATE too expensive >1 Gb/s (hundreds of I/Os)
  - DDR used widely for chip-to-chip in 3D; at rapidly increasing speeds
General I/O

- **Key specifications** (<100 Mb/s per pin)
  - $I_{IL}, I_{IH} < 10 \mu A$
  - $V_{OL}/I_{OL}, V_{OH}/I_{OL} < 50 \Omega$
  - Slew rate limiting
  - Setup/hold time

- **DFT techniques**
  - Boundary scan
  - All I/Os bidirectional

- **BIST techniques**
  - Programmable pull-up/down; test that it overdrives leakage
  - Adjustable boundary scan update ➔ capture timing

- **Most common technique**
  - Bidirectional I/O + boundary scan

- **Emerging problems**
  - Testing I/O connections on increasingly dense boards
  - Boundary scan may be too intrusive when 1000s of TSVs
  - Testing TSV quality

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Mentor’s IOTest™

- Measures delays
  - I/O wrap, rising, falling
  - SSN, rise/fall mismatch, pin-to-pin mismatch

- Unlimited time-resolution analysis (ns~ps)
  - Uses async clock from PLL for capture
  - No calibration or sensitivity to PVT
  - No changes to boundary scan cells
  - Suitable for all I/Os, including DDR

- Shifts out measured values, or pass/fail vs. per-pin limits
  - Measure any number of pins simultaneously

- RTL-synthesized, purely digital

US patents: 7453255, others pending
Sunter & Tilmann, "BIST of I/O circuit parameters via standard boundary scan", Int'l Test Conf., 2010

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ADC/ DAC

- Key specifications
  - DNL, INL <1 LSB
  - Aperture jitter <1 LSB equiv. (<2 ps rms)
  - SFDR >6 dB/bit
  - SNR >5 dB/bit

- DFT techniques
  - Scan access to digital; analog bus access to analog
  - Loopback, with offset voltage injection

- BIST techniques
  - On-chip linear ramp generation (~10 bits linearity)
  - Use DSP to perform FFT

- Most common technique
  - Functional testing by ATE

- Emerging problems
  - Embedded flash & large RAM >1 minute test – need multi-site test
  - Too many converters for ATE (10~100), especially if multi-site

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Random analog

- **Key specifications**
  - Slew rate
  - Overshoot
  - PSRR
  - Gain
  - DC voltage
  - etc.

- **DFT techniques**
  - Scan access to digital; analog bus (or multiplexer) access to analog
  - Ad hoc

- **BIST techniques**
  - Ad hoc

- **Most common technique**
  - Functional testing by ATE, via analog bus

- **Emerging problems**
  - Too many functions for ad hoc approach; unpredictable TTM
  - Too little reuse of solutions; no standards
  - Insufficient engineers with analog test skills

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F. Poehl et al., "Production test challenges for highly integrated mobile phone SoCs - A case study", Eur. Test Symp. 2010

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Mentor’s Analog DFT/ BI ST (in development)

Three principles
- Unlimited voltage resolution: PWM, sigma-delta, oversampling
- Unlimited time resolution: undersampling periodic signals
- Unlimited number of nodes: 2 shift registers, 1687-like addressing

Four building blocks
- Shared digital stimulus generation + stimulus shift reg.
  - Clock-like waveform, PWM, sigma-delta, ...
- Simple D/A conversion
  - No need to test it, eg. RC
- Simple A/D conversion
  - No need to test it, eg. sampling comparator
- Response shift reg. + shared digital response analysis
  - Accumulator, timing analyser, DSP, ...

Serial digital version of 1149.4

RF analog

- Key specifications
  - Third-order intercept
  - Output power
  - Bandwidth, frequency
  - Noise

- DFT techniques
  - Analog bus to monitor $V_{BIAS}$
  - Analog bus to monitor power detector $V_{DC}$
  - Down-mixer

- BIST techniques
  - Loopback

- Most common technique
  - Functional testing by ATE

- Emerging problems
  - Crosstalk between radios of a chip
  - Crosstalk during multi-site test

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Zhang et al., "Low Cost RF Receiver Parameter Measurement with On-chip Amplitude Detectors", VLSI Test Symp., 2008

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Conclusions

■ 3D packaging introduces test problems
  — KGD, less access, more I/Os, interconnect yield

■ DFT standards mostly applicable to digital test
  — 1149.1, 1149.6, 1149.7, 1500, P1687
  — 1149.4 has many limitations due to its analog nature

■ Varying amounts of DFT/BIST adoption in industry
  — PLL
  — SerDes
  — DDR I/Os
  — General I/Os
  — ADC/DAC
  — Analog
  — RF

■ Mentor is the only company providing general DFT/BIST solutions