



SYSTEM-ON-CHIP RESEARCH NETWORK



Registered clients of CMC can access the design files and documentation described below from the CMC Technology Gateway at: <https://www2.cmc.ca:2804/> (use the Search function)

All trademarks are the property of their respective owners **NEW!** Indicates new since October 2006

NEW! Multiprocessor SOC for FPGA and Simulation

Description: Includes four microblaze microprocessors (with BRAM), DDR SDRAM, two UARTs and other components. Communication between microblaze processors is through a FSL (Fast Simplex Link) channel, with parallel image processing. This system can be implemented in two ways:

1. In a StepNP SystemC simulation environment
2. On the FPGA housed in the AMIRIX AP1000 board

The release includes design files, installation instructions and tutorials for both approaches.

NEW! Celoxica C-Based Hardware Design Tool, DK

Description: Allows researchers to design and implement hardware using a C-based language, instead of relying on a low-level language such as VHDL or Verilog. The release from CMC includes:

- DK Design Suite
- PDK (Platform Development Kit)
- Two RC10 FPGA prototyping boards per site license

Availability: Tools have been distributed to 22 universities.

Tensilica Xtensa LX Configurable Processor: FPGA Implementation Service

Description: A service for university researchers to access hardware implementations (targeting Xilinx FPGAs) of the Tensilica Xtensa LX configurable processor technology. This technology is suitable for prototyping designs with low-power applications.

Also available from the CMC Technology Gateway: design example, reference design (**NEW!**), and documentation to help users implement the hardware and software of a Tensilica Xtensa LX-based SOC design on the AMIRIX AP1000 platform.

Availability: To access the online request form visit <https://www1.cmc.ca/subscribers/design/soc/tensilica.php>

Prototyping Station Using the Virtex-II Pro FPGA (AMIRIX)

Description: Based on the Xilinx Virtex-II Pro FPGA. Includes an AMIRIX AP1000 development board installed in the 64-bit PCI-X slot of an IBM Intellistation Z Pro workstation. With large FPGA gate capacity (44000 logic slices) and two embedded IBM PowerPC hard macros, as well as up to 1.4MB of on-chip RAM, this platform gives university researchers a high-performance, multiprocessor development environment. Supported by getting started documentation, application notes, and design examples.

NEW! An application note with design example that demonstrates how to generate a hardware design language (HDL) system block from your MATLAB design file using the Xilinx AccelDSP tool, and incorporate it with other system blocks.

Availability: 230 stations have been deployed to 35 universities.

System-Level Prototyping Station (SLPS)

Description: Set of three FPGA prototyping systems targeting DSP, embedded systems, and multimedia research. Each station includes a development board (Altera or Xilinx), PC-based CAD environment (including Matlab/Simulink, and Mentor Graphics' FPGA Advantage tool suite, which includes ModelSim simulator and Precision RTL synthesis tool), and PC (acting as host PC for both the CAD environment and the development board). Supported by getting started documentation, application notes, and design examples. Also available: Embedded Linux OS, tutorials and design examples; Embedded Linux for both Nios II and MicroBlaze systems.

NEW! Design files and documentation that provide:

- Wireless Ethernet connectivity for embedded solutions
- Capability to add Ethernet functionality and USB host/slave functionality to a Nios II system

Availability: 430 SLPS systems have been distributed to nearly 30 universities.

CoWare System-Level Tools

Description: Platform Architect (SystemC-based design environment, including model libraries, for simulation, debug and analysis of system architectures); Processor Designer (design and implementation of application-specific processors); and Signal Processing Designer (block-based graphical design and simulation environment for DSP-based systems).

Forte Synthesizer

Description: Behavioural synthesis of transaction-level models (TLM) in SystemC to RTL, targeting FPGA and ASIC hardware implementation.

StepNP Simulation Platform

Description: A multi-processor simulation platform targeting networking applications. It includes HW SystemC models (processor, memory, bus, etc.), SOC GUI tool for simulation analysis and display, and networking application software. Created by STMicroelectronics and donated for research at Canadian universities. Includes tutorial, reference manual and user guide documentation to reduce the learning curve for users.

Embedded Linux

Description: Design files, application notes, user documentation and tutorials for creating and using the Embedded Linux OS kernel on CMC's supported processors. Includes Embedded Linux for Altera Nios II (including tutorial), Xilinx MicroBlaze, Amirix AP1000 board with PPC405 processor, and ARM Integrator/CM7TDMI.

Embedded Software Design

Description: Tools, flow, and documentation to create embedded software for systems based on the architectures that CMC supports (ARM7, Nios II, Microblaze, PPC405 and Tensilica). Tools include the ARM Developer Suite (ADS), Xilinx's EDK, Altera's Nios II IDE, ELDK for PPC, Tensilica's Xtensa Xplorer, Mentor's XRAY Debugger, Telelogic's Tau (SDL and UML design) and Mentor's Seamless CVE (SW/HW co-simulation). Supporting material includes documents on the development flow, porting an RTOS to a customized platform in Seamless CVE, and Embedded Linux for all CMC supported processors (see above).

SOC Physical Design Environment

Description: Libraries and IP for large digital chip design, including Cadence's First Encounter (floorplanning), CeltIC (signal integrity) and Digital Design Environment (SOC design methodology based on Tality flows, instructional materials, million-gate example design with AMBA bus, AMBA Transactional Verification Models and Verification Reuse Methodology), Synopsys PrimeTime (static timing analysis) and Formality (equivalency checking), Artisan Components standard cell libraries for TSMC's 0.18-micron CMOS.

Physical Design Environment

Description: Best-in-class tools from Cadence, Synopsys, and Mentor Graphics to design components (digital, mixed-signal, RF, analog, MEMS) across a number of technologies (e.g., 90nm, 180nm and 350nm CMOS). Capabilities include design entry, synthesis, place-and-route, simulation, design rule checking (DRC), timing analysis, and so on.

Availability: CAD tools are delivered through the Sustainable Technology Configuration (STC) environment. Licenses are updated and delivered on a yearly basis.

Hardware/Software Co-Verification

Description: Mentor Graphics' Seamless enables instruction-set simulation of system software alongside a hardware simulation of the system architecture. Supported with the ARM7TDMI processor support package (PSP) and Cadence Design System's NC-Sim simulator.

IP Block Authoring Flow (Documentation and Design Example)

Description: Demonstrates coding standards and tool use for creating reusable digital IP blocks.

Silicon SOC Platform

Description: RTL-based SOC Platform (Tality Bluetooth SOC Integration Platform) includes the Bluetooth baseband core, ARM7TDMI hard macro, AMBA bus and peripherals, Bluetooth protocol stack and application profiles, analog blocks (PLL and oscillator), and Virage memory cores.

ARM7TDMI Microprocessor Core

Description: Hard macro form of the ARM7TDMI microprocessor, including design footprints, timing models, test vectors, and example AMBA system design.

Memory Integration Application Note

Description: A basic flow and design example that demonstrates how to generate and integrate a Virage Logic memory core with design blocks. The release includes an introduction to the models required for the integration flow, a generic design flow using the Virage memory compiler, an explanation of the design flow steps, and a design example that demonstrates the memory integration flow. The design flow incorporates simulation tools from Cadence, Synopsys and Virage Logic, as well as Unix automation tools (i.e., 'make').

For further information contact Hugh Pollitt-Smith, CMC Microsystems, 613.530.4668, pollitt-smith@cmc.ca