Join us to help specify the technology attributes of your research platforms.

University faculty, graduate students, and engineers & managers at companies from all industrial sectors are invited to a platform technology planning and forecasting session co-located with the CMC/ITAC annual symposium October 15 and 16, 2013. This informal 2-hour session on October 15 at 13:30 open to general Symposium registrants will explore options for the specification and development of heterogeneous computing R&D platforms comprised of high performance CPUs, many-core CPU fabrics, GP-GPU, FPGA, custom hardware accelerators, high speed interconnect, run-time environments, and parallel programming paradigms. The outcome of the session will in part guide procurement in 2014-15 of prototyping platforms for delivery to embedded system researchers in Canada’s National Design Network (NDN). These are used by faculty, graduate students and their industrial collaborators who have interests in architecture exploration, algorithm mapping, embedded software development/parallelization, performance/power optimization, reliability, and debug. Topics include the merits and futures of C, C++, System C, OpenCL, NOCs, QPI, PCI-E, RTL synthesizable platforms, virtual platforms, Virtex, Stratix, Xeon E5, Fusion, Tilera, Vocallo, Xeon Phi, Tesla Kepler, etc. Attendees will be expected to participate!

Meeting objective: Capture heterogeneous platform specifications for 2014-15 procurements and preliminary work on new NDN proposals

Agenda
1. Quick overview on the National Design Network and CMC support for research and startups
2. Embedded system research topics: discussion and feedback
3. Platform attributes in support of the research: discussion and feedback

No additional registration required.

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