Course Specification

DSP Design Using System Generator
DSP 3

Course Description
This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware co-simulation verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification using the Xilinx FPGA capabilities.

Lab Descriptions

Lab 1: Using the Simulink Software – Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.

Lab 2: Getting Started with Xilinx System Generator – Illustrates a DSP48-based design. Perform hardware co-simulation verification targeting a Xilinx evaluation board.

Lab 3: Signal Routing – Design padding and unpadding logic by using signal routing blocks.

Lab 4: Implementing System Control – Design an address generator circuit by using blocks and Mcode.

Lab 5: Designing a MAC-Based FIR – Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware co-simulation by using a Xilinx evaluation board.

Lab 6: Designing a FIR Filter Using the FIR Compiler Block – Design a bandpass FIR filter by using the FIR Compiler block to demonstrate increased productivity. Verify the design through hardware co-simulation by using a Xilinx evaluation board.

Lab 7: System Generator and Project Navigator Integration – Learn how to embed two System Generator designs into a larger design and how VHDL created by System Generator can be incorporated into the simulation model of the overall system.

Lab 8: Using System Generator to Develop Virtex-6 and Spartan-6 FPGA DSP Applications – Design a single-carrier Digital Up Converter (DUC) and Digital Down Converter (DDC) to meet WCDMA UMTS 3GPP specifications.

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