CMC MICROSYSTEMS

# Webinar

## Introduction to the HPP-Heterogeneous Processing Platform

*A combination of Multi-core, GPUs, FPGAs and Many-core accelerators*

To hear the audio, please be sure to dial in: 1-866-440-4486 ID# 4503739


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15-10-2013

# Agenda

- Introduction
- emSYSCAN Development Systems Update
- Processor Eras : Historical background
- HPP-Heterogenous Processing Platform
  - Hardware architecture
  - Software architecture
- Research topics enabled
- Getting Started with the HPP
- Live demo
- HPP Roadmap
- Discussion

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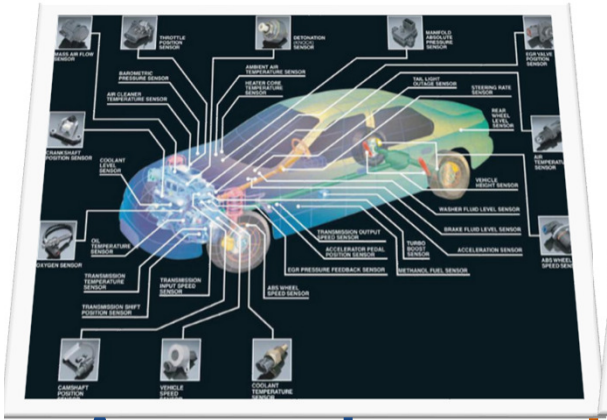
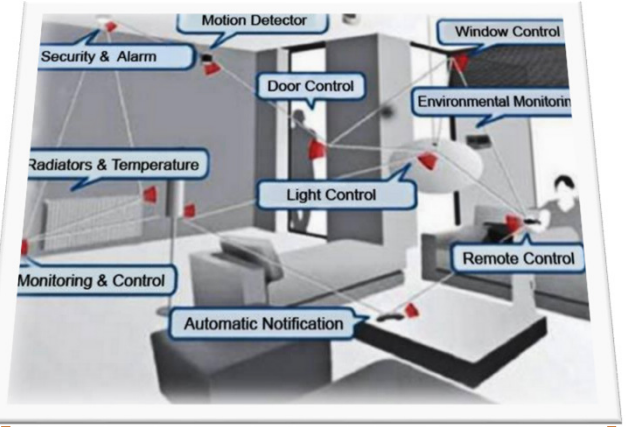
# PROCESSOR ERAS : HISTORICAL BACKGROUND

# Multicore processors
# Further growth of established markets

- Multiprocessors are used everywhere



Automotive



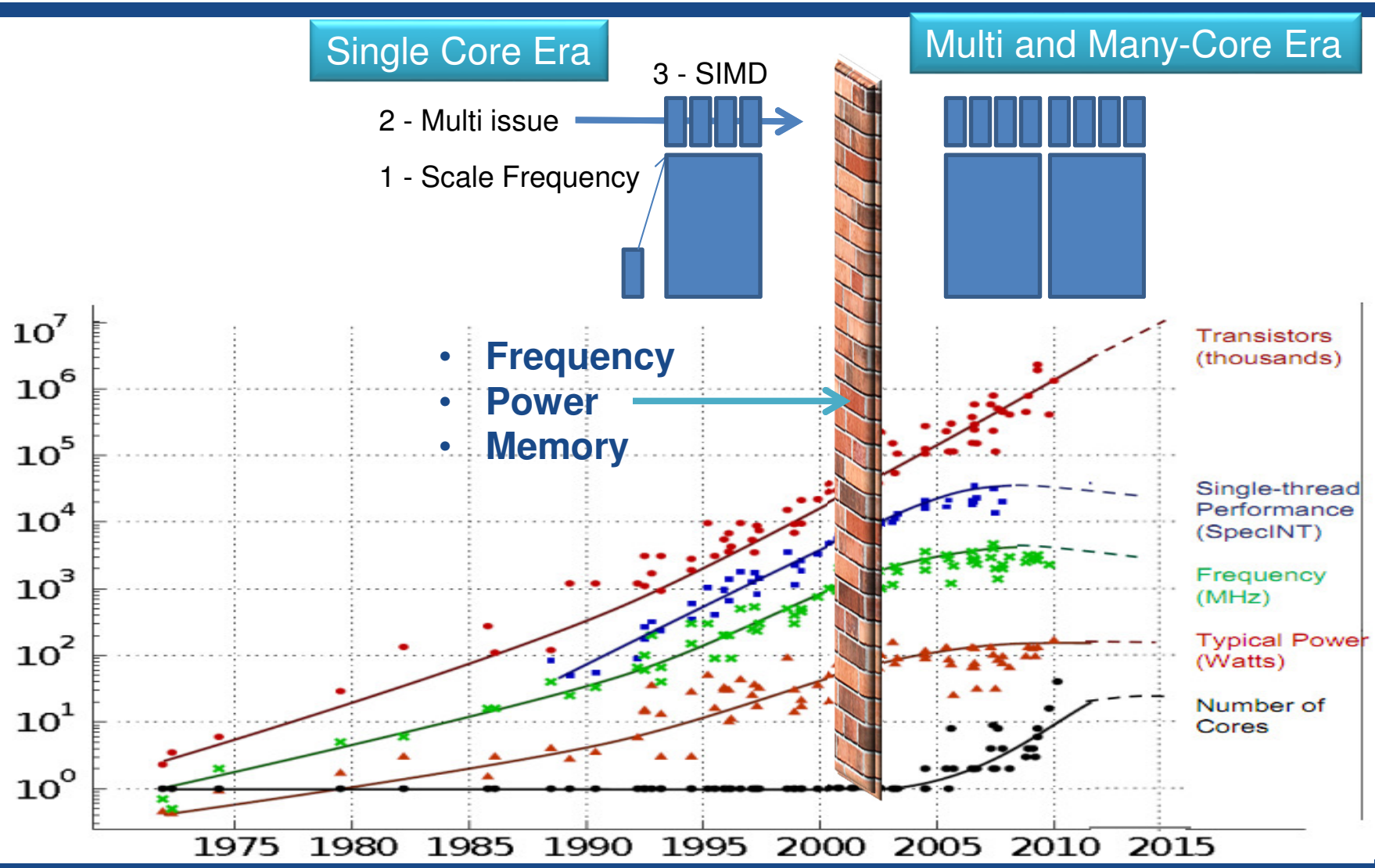

Home sensor network

Mobiles

Desktops

HPC

# 35 YEARS OF MICROPROCESSOR TREND DATA




Original data collected and plotted by :
M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten Dotted line extrapolations by C. Moor

# Three Eras of Processor Performance

## Single-Core Era

**Enabled by**

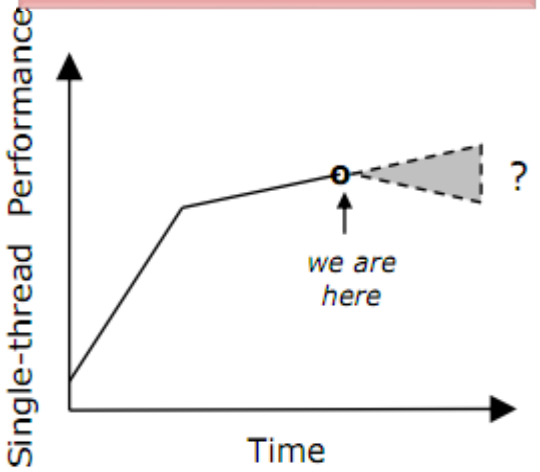
- Moore's Law
- Voltage Scaling
- Microarchitecture

**Constrained by**

X **Power**

X Complexity

Assembly>C>C++,Java




## Multi-Many Core Era

**Enabled by**

- Moore's Law
- Desire for throughput
- Desire for performance

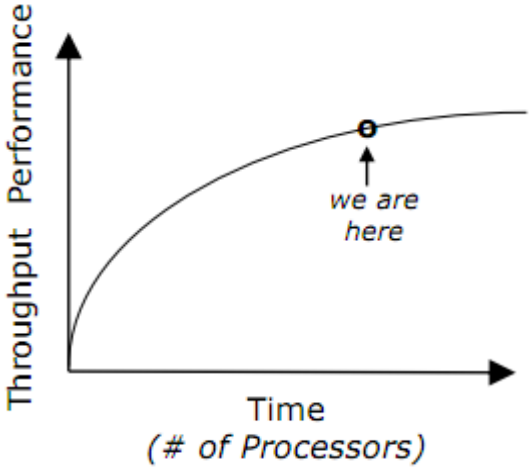
**Constrained by**

X **Power**

X Parallel SW availability

X Scalability

Pthreads>OpenMP/TBB




## Heterogeneous Systems Era

Enabled by

- Moore's Law
- Abundant data parallelism
- Power efficient GPUs

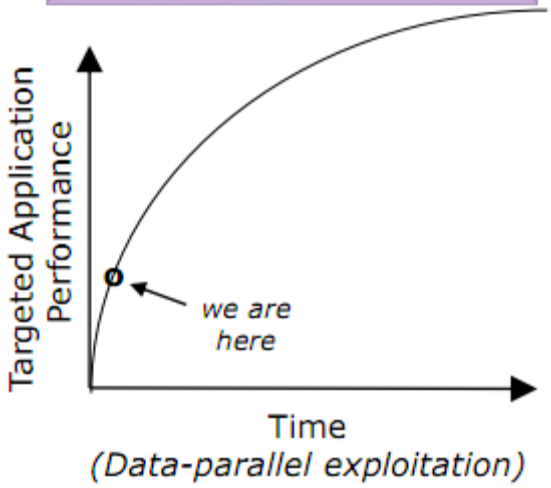
**Constrained by**

X **Power**

**X Programming models**

X Communication overheads

Shader>Cuda>OpenCL




Source : The Salishan Conference on High Speed Computing, DATA PROCESSING IN EXASCALE-CLASS COMPUTER SYSTEMS Chuck Moore AMD Corporate Fellow & Technology Group CTO

# Heterogeneous environment

## Software applications

## Software stack

**Programming models APIs**

- Extended OS API
- Legacy API
- Application Specific API

**Tools and Compilers**

- Parallelizers
- Compilers
- Debug
- Trace

**OSes, Runtimes, Drivers**

- Real-time
- GP OS
- Special OS

## Hardware

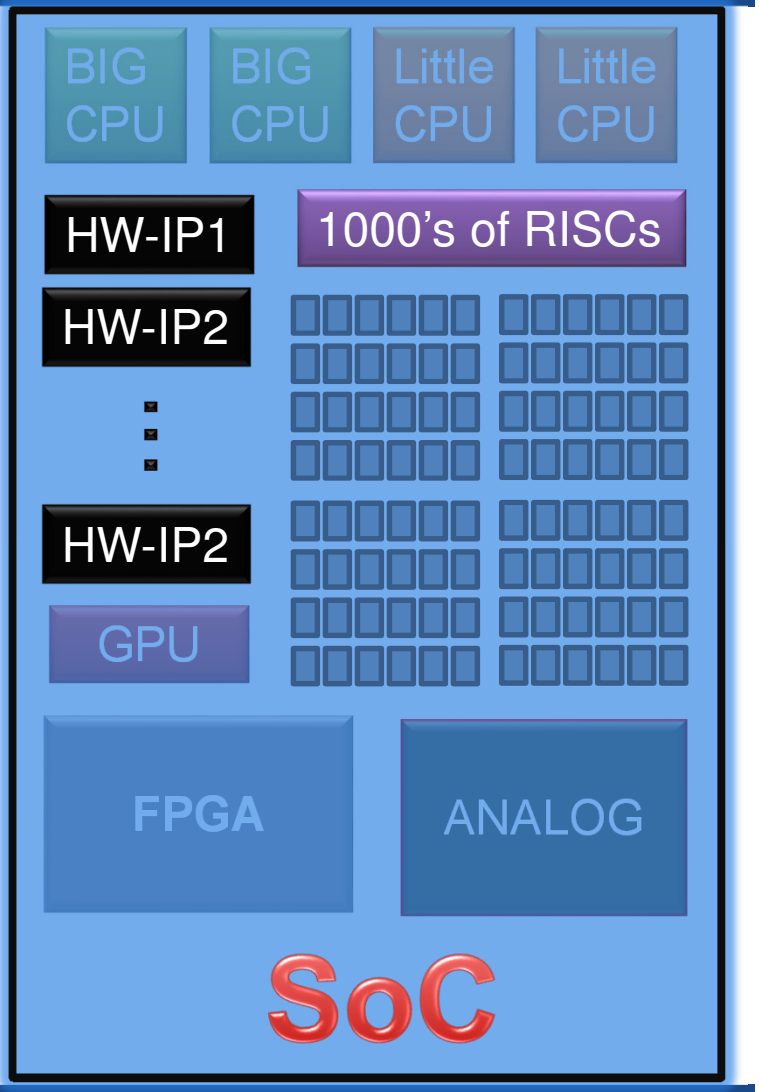
- Multi-core
- GPU
- FPGA
- ASIC

# A heterogeneous landscape

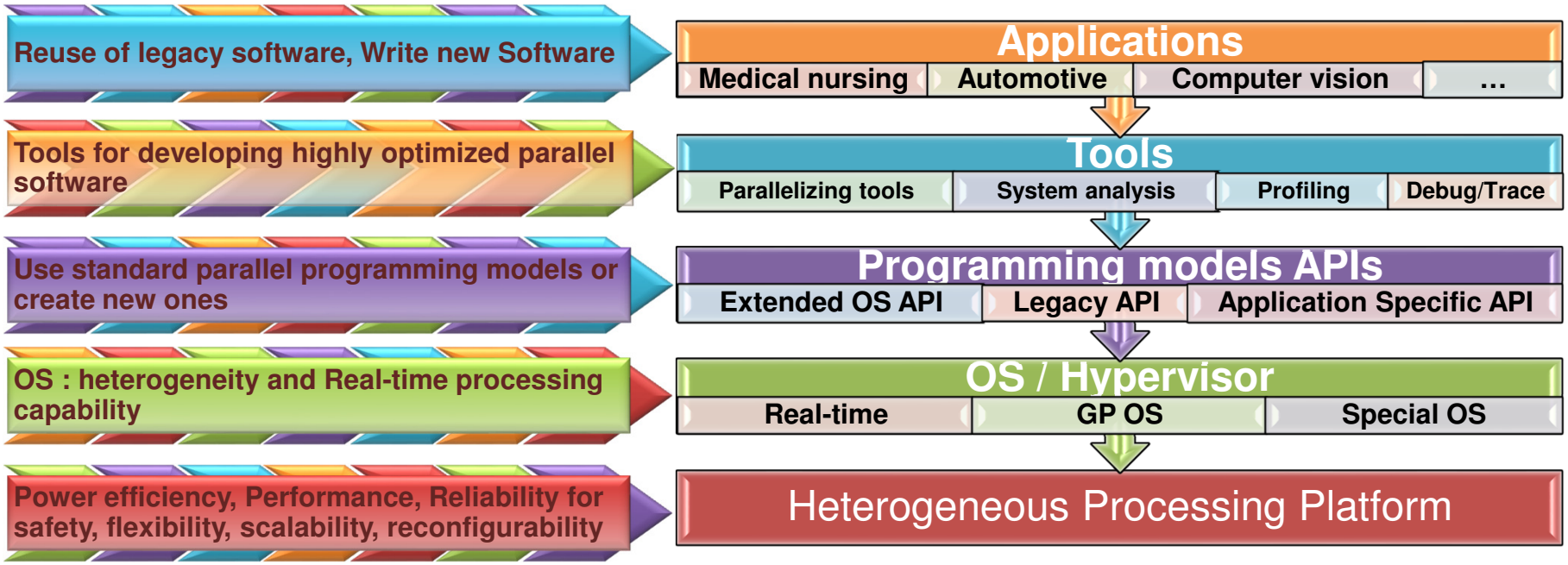
- **Integration of different type of compute units:**
  - Big CPUs, Little CPUs
  - GPU
  - FPGA
  - 1000's of RISC processors

- **Examples:**
  - ARM : Big Little
  - Xilinx : Zynq
  - Qualcomm : Snap dragon

- **Serious software challenge:**
  - How to program a heterogeneous computing fabric ?



# Heterogeneous Systems
## Software Stack

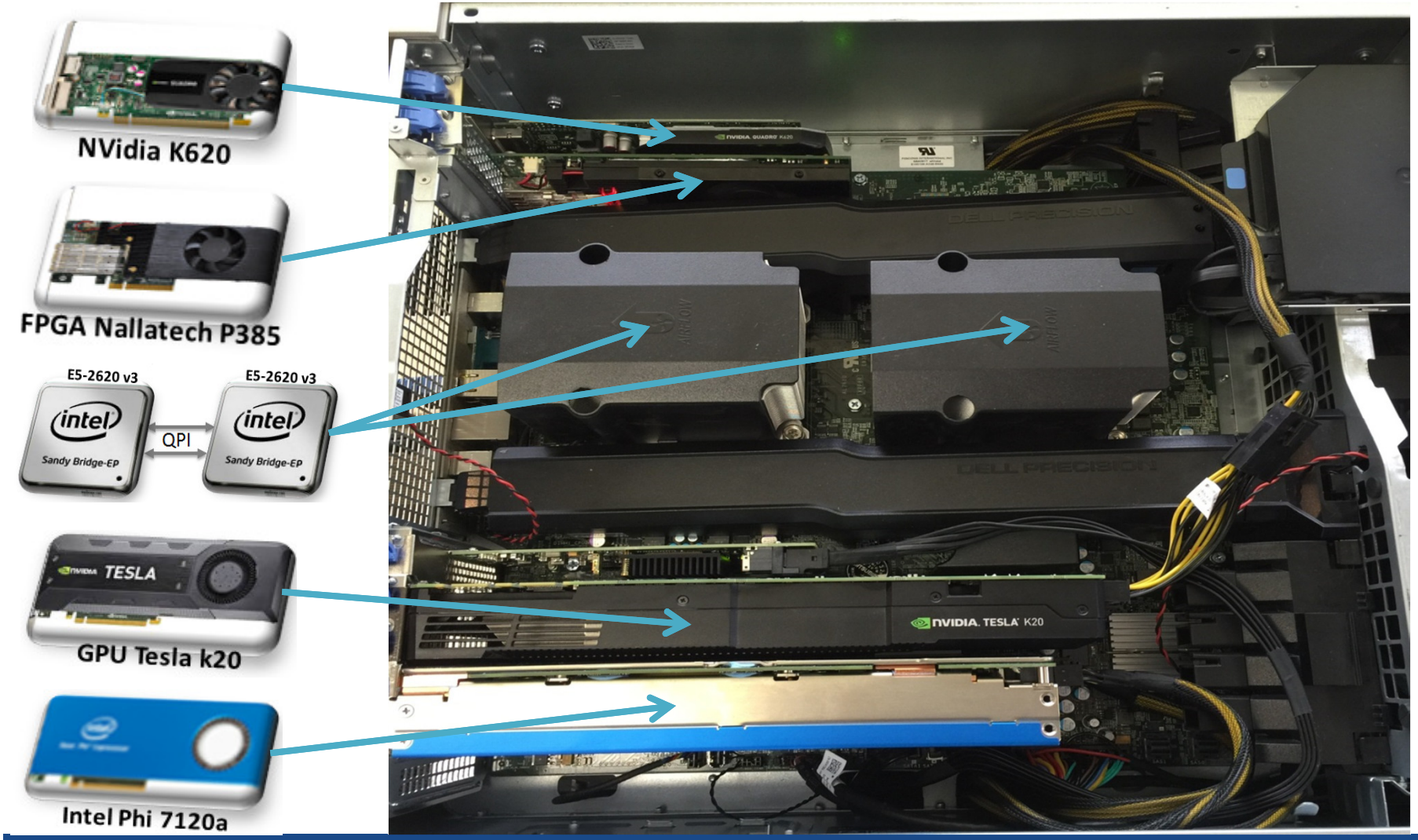


# HPP HARDWARE ARCHITECTURE

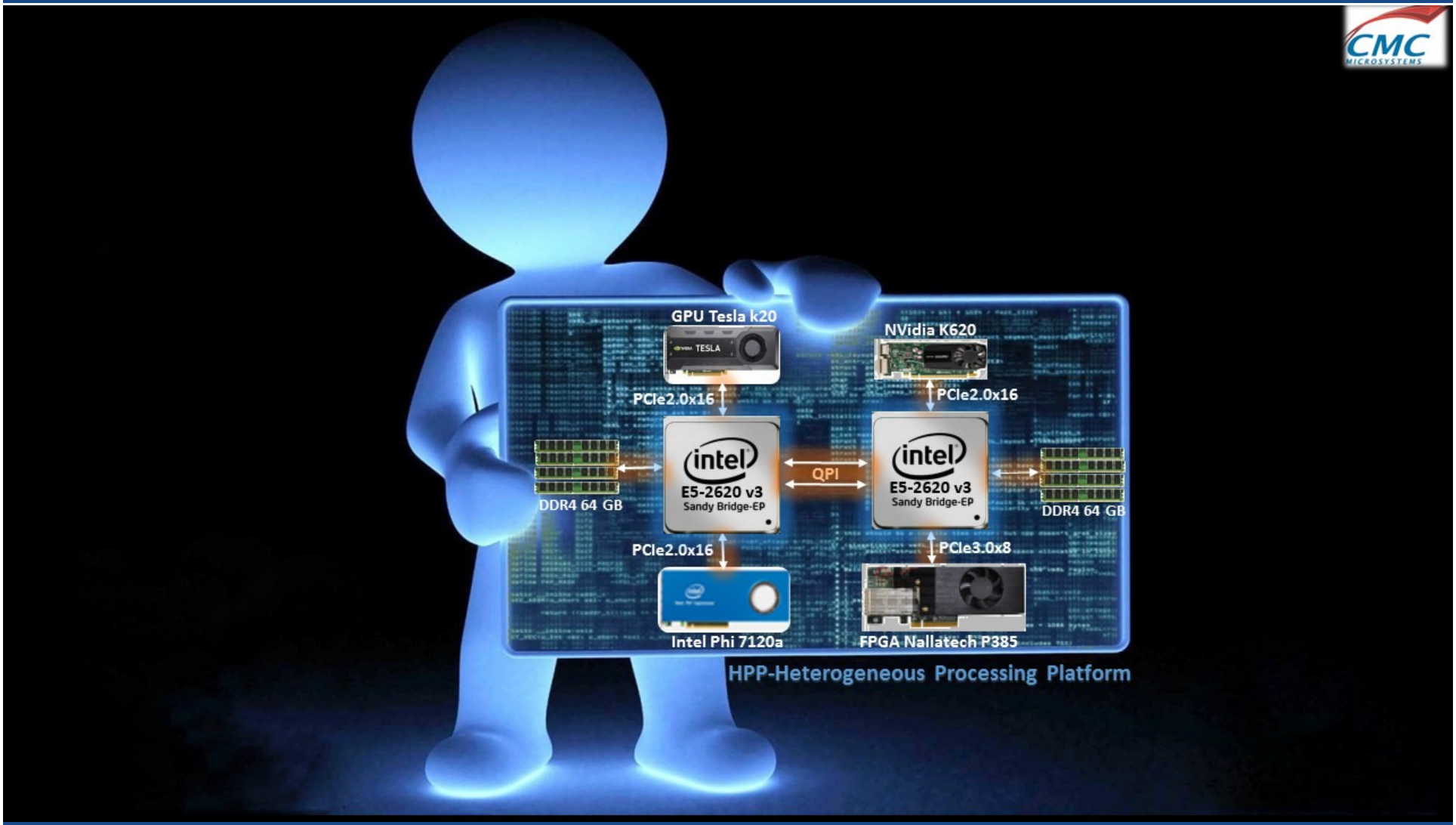
# HPP main components

- The HPP workstation integrates the following main components:
  - Dual core Intel Xeon E5-2620 V3
  - NVidia GPU (Tesla K20)
  - FPGA board (Nallatech P385-A72).
  - Xeon Phi 7120A
- Key Platform Benefits
  - Customizability: Select the right mix of accelerators for your application
  - Greater flexibility for HW/SW exploration
  - Scalability: Create one node and scale up by adding more nodes
  - Fast automated setup and configuration
  - Technical support and training from CMC Microsystems

# HPP fully installed system



# HPP wallpaper



# HPP workstation

| | |
|---|---|
| **Processor/Cache** | |
| **CPU** | 2 x Intel® Xeon® Processor E5-2620 Series, v3, (6 cores, 85w) |
| **CPU Cache** | 15MB / Processor |
| **System Memory** | |
| **System Memory** | 128GB ECC, 2133MHz DDR4 RDIMM |
| **Expansion Slots** | |
| **PCI-Express** | 2 PCI-E 3.0 x16 double-wide form factor<br><br>2 PCI-E 3.0 x8 half-height, half-length single-width |
| **Network and Video** | |
| **Network Controllers** | Intel i217 Digabit Ethernet |
| **Video** | Nvidia k620 2 GB |
| **Power Supply** | |
| **1300W power supply, 120 VAC 60Hz UL/CSA power source“** | |
| **Storage** | |
| **500 GB SATA 1st Solid state (SSD)** | |
| **1TB SATA 7200 2nd HDD** | |
| **DVD-R/W** | |
| **System/CPU cooling** | |
| **Other Features** | |
| **USB Keyboard and Mouse** | |
| **3-year parts and labour Canada-wide on-site warranty service (9:00am-5:00pm, Monday-Friday)** | |
| **22” LCD Monitor; 1920 x 1080 resolution connected via DVI or HDMI** | |

# HPP Accelerators


| Accelerator | Features | Host interface | Compute performance | Power |
|---|---|---|---|---|
| **Nallatech 385** | Altera Stratix V<br>Mem. 2 banks of 4GB | PCIe 3.0 x 8 | unavailable | Typical application ≤ 25W |
| **TESLA K20** | 2496 CUDA cores<br>5GB 208 GB/s | PCIe 2.0 x 16 | 3.52 TFLOPS (single precision) 1.17 TFLOPs (double precision) | 225W |
| **Xeon Phi 7120a** | 61 Cores, 1.33 GHz<br>Mem. 16GB at 352 Gb/sec | PCIe 2.0 x 16 | Peak Double Precision 1.003 TFLOPs | 300W |


# HPP SOFTWARE ARCHITECTURE

# HPP Pre-Installed Software Components


These software components required by the HPP are pre-installed on the workstation:

- RedHat Enterprise Linux 6.6 (Kernel version: 2.6.32-504.el6.x86_64)
- Java Runtime Environment (JRE)
- gcc compiler and toolchain

| Accelerator | Software and tools |
|---|---|
| **GPU Tesla K20** | • NVIDIA CUDA 7 Toolkit |
| **Nallatech FPGA P385** | • Altera Quartus 15.0, Altera SDK for OpenCL 1.0<br>• Nallatech FPGA P385 Board Support Package |
| **Xeon Phi 7120a** | • Intel Manycore Platform Software Stack (MPSS) 3.5.1 for Linux<br>• Intel Parallel Studio XE 2015, Professional Studio for C++, Linux version<br>  ○ Intel C++/C/FORTRAN compilers, Intel Math Kernel Library<br>  ○ Debuggers, Performance and Correctness Analysis Tools<br>  ○ OpenMP, MPI, OFED messaging infrastructure (Linux only), OpenCL<br>  ○ Programming Models: Offload, Native and mixed Offload+Native |

# Research topics enabled


Research Topics targeting parallel embedded systems:

- **Software IPs and applications** targeting heterogeneous parallel systems (e.g. imaging, video, and next-generation immersive applications such as computational photography and augmented reality)
- **Software stack**
  - Parallel programming models, Compilers, middleware, Runtime, drivers and OSes
- **Heterogeneous parallel architecture**
  - Hardware/Software exploration
  - Debug and trace of applications running on a heterogeneous parallel system

# GETTING STARTED WITH THE HPP

# HPP Remote Access

- **In order to install the VNC server on the HPP system, enter the following command in a terminal:**

  *# yum install tigervnc-server*

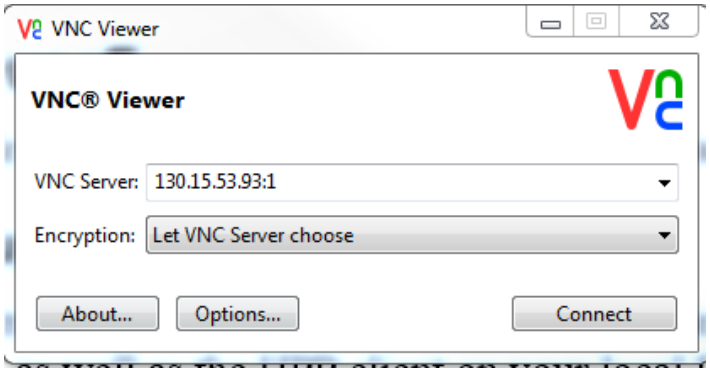
- **In order to start a VNC session on the HPP, enter the following command in a terminal:**

  *# vncserver -depth 24 -geometry 1680x1050*

- **Note: The optimal values for the geometry setting depends on your screen size and resolution. The output of this command will include a line similar to the following:**

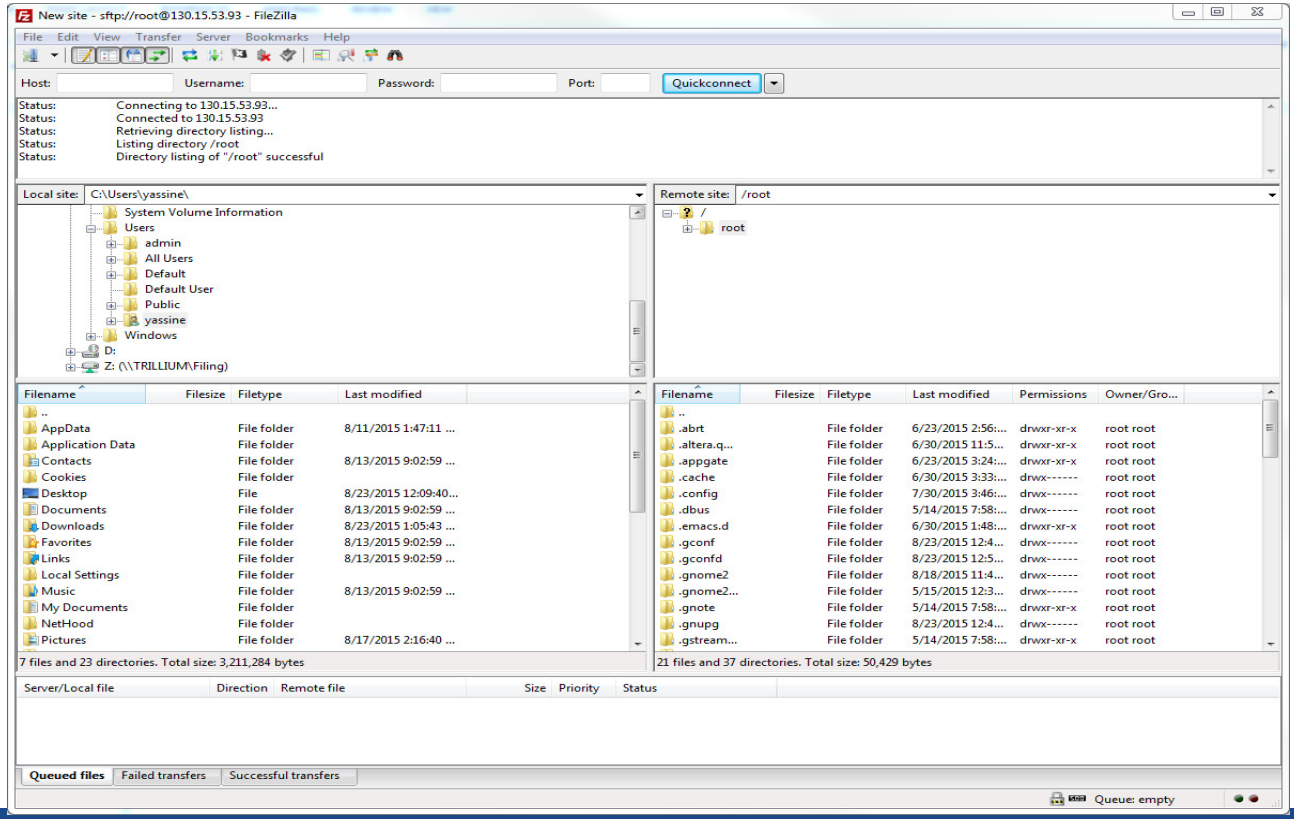
  *New 'HPPPrototype:# (root)' desktop is HPPPrototype:#*

  *Starting applications specified in /root/.vnc/xstartup*



# Transferring Files To or From the HPP System

- FileZilla is an open source, GUI-based client application for Windows and Linux available for free from http://filezilla-project.org/. To connect to the HPP sftp site using FileZilla, perform the following tasks:
  1. From the field Host, enter the IP address of your HPP system.
  2. From the fields Username and Password, enter your HPP user ID and password, respectively.
  3. Select SFTP in the protocol field
  4. Leave the Port field blank.
  5. Click Connect.



# Setting up Altera Design Tools License using CADpass

- CADpass on Linux platforms is required to run Altera tools. In order to use the Altera design tools, you need to launch CADpass from the CMC web portal by performing the following tasks:
  - Right-click on "agclient.jnlp" located at: /CMC/tools.
  - From the menu, select: Open with> IcedTea Web Start.
  - Click Allow in the security window.
  - Enter your CMC subscription: email address and password.
  - Select Altera tool by double clicking Altera icon from the tools list

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# LIVE DEMO

# HPP Roadmap


Status (12 universities selected 18 systems G1, 7 universities selected 8 G2)

- Assembled, cloned and tested 18/18 units. Shipping is in progress…

User Guides

- (1) Quick start guide : Heterogeneous Parallel Platform (HPP) (to be released next week)
- (2) User Guide: Performance and Power profiling for the HPP (In progress)

Webinars series for the HPP

- Introduction to the HPP-Heterogeneous Parallel Platform: A combination of Multicores, GPUs, FPGAs and Many-cores accelerators (August 26th)
- Programming models, performance and power profiling for the HPP-Heterogeneous Parallel Platform (October)
- Computer vision using OpenCV/OpenCL targeting the HPP- Heterogeneous Processing Platform (November)

HPP Workshops (November)

- User group workshop: presentations/demo/discussion
- Training: tools and programming models for the HPP

# DISCUSSION