Silicon photonic gyroscope validation using the Microsystems Integration Platform

April 8, 2014

Silicon photonic gyroscope validation using the Microsystem Integration Platform

- What is the MIP?
- Introduction to the MIP variant for Si-Photonic Hardware in the Loop
- Si-photonics background: Design, fabrication, test, training
- Reference Design: Application to Si-P gyroscope validation
- MIP generation 2 rollout: How can I get one?

- Miguel Torres, Lukas Chrostowski, Edmond Cretu, Nicolas Jaeger
  - Department of Electrical and Computer Engineering
- Robert Mallard
  - Optoelectronic Engineering, CMC

emSYSCAN

Microsystems Rapid-Prototyping, Characterization and Integration Labs

4 Universities:
- UBC
- U Manitoba
- Queen's
- École Polytechnique

- Minimized development cycle prototyping and performance measurement
- Integration for field testing

All 37 Universities

Multi-Technology Design Environment
- System architecture exploration
- Multi-technology simulation
- Design of custom devices for manufacturing

Development Systems
- System validation and proof-of-concept demonstration

License Management Appliance

Installed Design Environment

Development System Hardware

Real-Time Embedded Software Lab

University of Waterloo

- Design, analysis, debug of real-time software on next-generation processor systems

Secure, Managed Access

Management & Operations
Includes selection; procurement; configuration; installation and delivery; access and utilization management; engineering/technical support; Train-the-Trainer events; emSYSCAN Advisory Group coordination; reporting, legal and financial administration.

License Management Server (LMS)

Microsystem Integration Platform Standard Implementation

The Microsystems Integration Platform (MIP) is a benchtop instrument intended for multi-technology validation of the functionality of a micro-device in a system context.

The list of MIP variants currently includes:

- Generic MEMS
- Microfluidics
- Micromirror
- RF-MEMS
- Si-photonic HW-in-the-loop

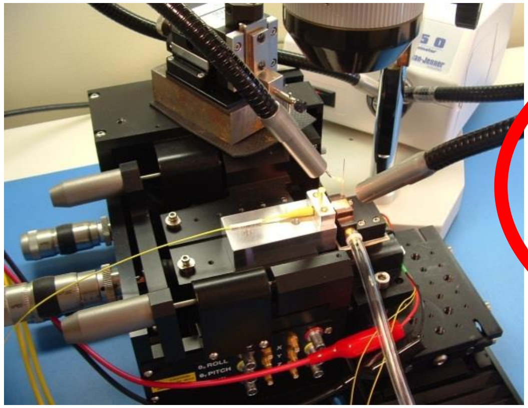
Information on the features and specifications of each of these variants may be found at:

http://www.cmc.ca/WhatWeOffer/Prototyping/MIP.aspx

Photonic MIP HW-in-the-loop

A system for:

- putting the optical device to work
- testing a microsystem employing optical technology



- **Real time control**
- **System operational algorithm exploration**

Photonic MIP HW-in-the-loop

http://www.cmc.ca/WhatWeOffer/Prototyping/MIP/Si-Photonic.aspx

Agilent C band tunable laser

Agilent 4 port optical power meter

MIP Hub
- Integrated design environment and programmable control
- Real time
- Embedded instrumentation

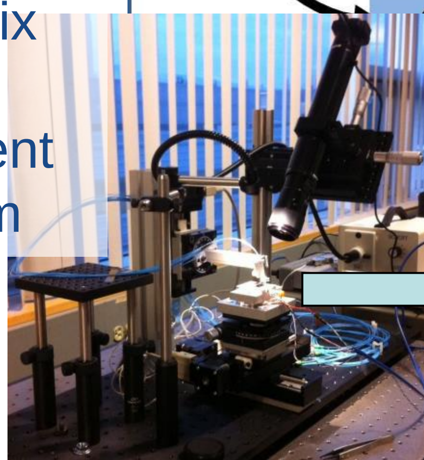
Optical source

Optical detection

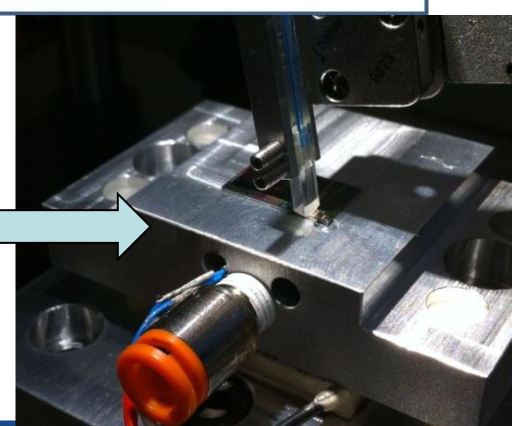
Automated optical alignment

Si-photonic HW in the loop

Custom Micronix auto-alignment system



Standard chip to verify optical coupling

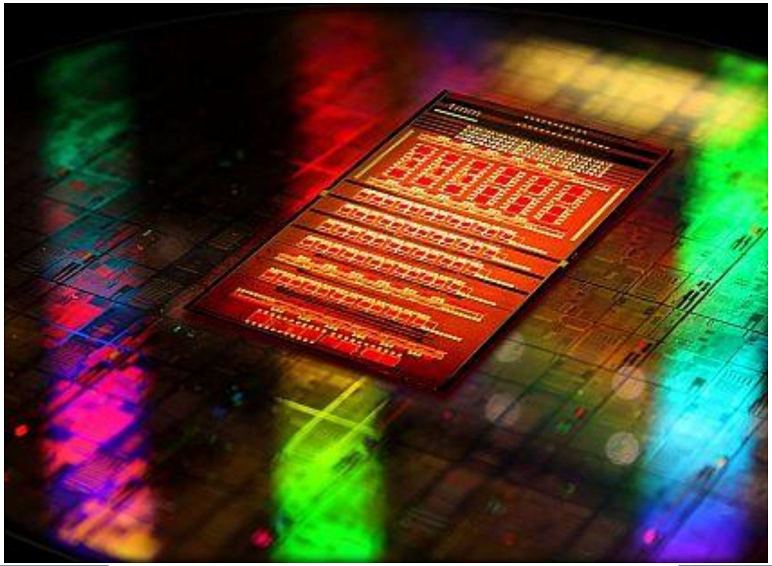


PLC Connections 8-element PM fibre coupler for surface gratings

Silicon Photonics

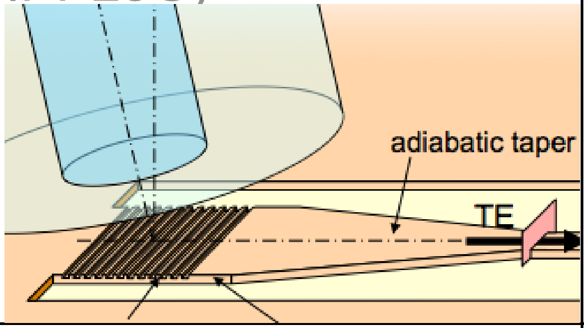
- Silicon electronics industry
  – $40+ Billion annual R&D investment*
  – Mature materials, **processing**, **design technologies**
  – Possibility of leveraging this technology for optics/photonics
- Silicon photonics
  – "integrated optics" and "photonic integrated circuits (PICs)" on silicon
  – use silicon as an optical waveguide material and for optical processing/switching
- supported by CMC:
  – Foundry fabrication
    - imec ePIXfab, IME, etc.
  – Si-EPIC training + fabrication workshops
    - Offered since 2007 – and growing
  – This Webinar – hardware for automated measurements
    - Variety of automated systems in use at UBC since 2010

IBM:

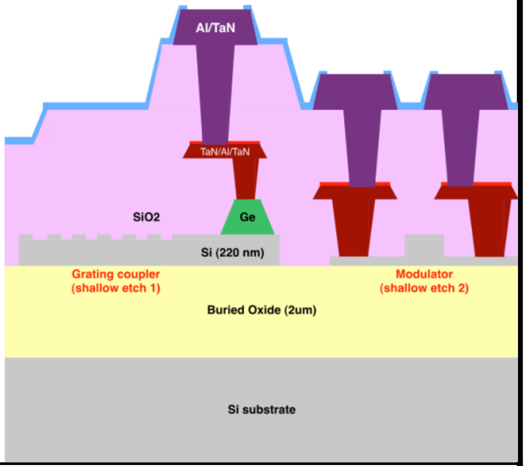


Fabless Fabrication via Foundries Multi-Project Wafers (MPW)

ePIXfab imec
- Passives, grating couplers
- Actives (ISIPP25G)



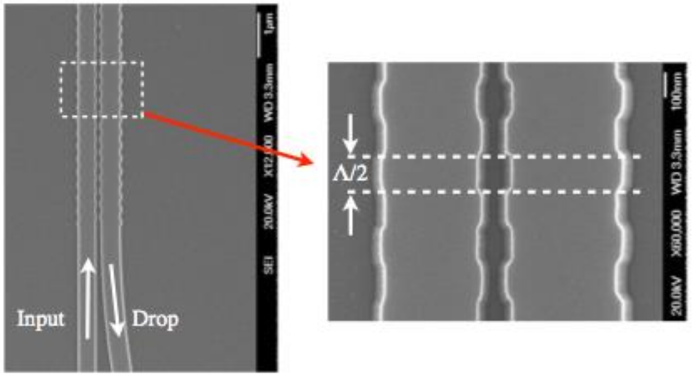
IME (OpSIS & CMC)
- Passives
- Modulators
- Detectors
- Edge / grating coupling



ePIXfab LETI
- new Full Platform

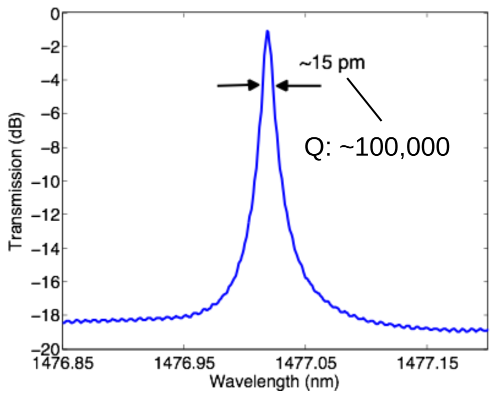
ePIXfab IHP
- passives
- …

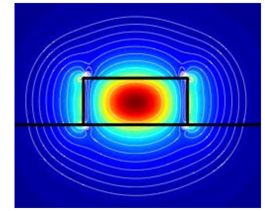
100 keV **E-Beam** Lithography Univ. Washington MFF

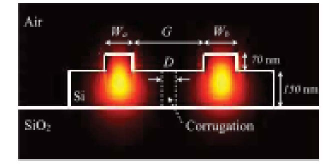


NSERC CREATE SiEPIC Program – Training for Research in silicon photonics

Design cycle:





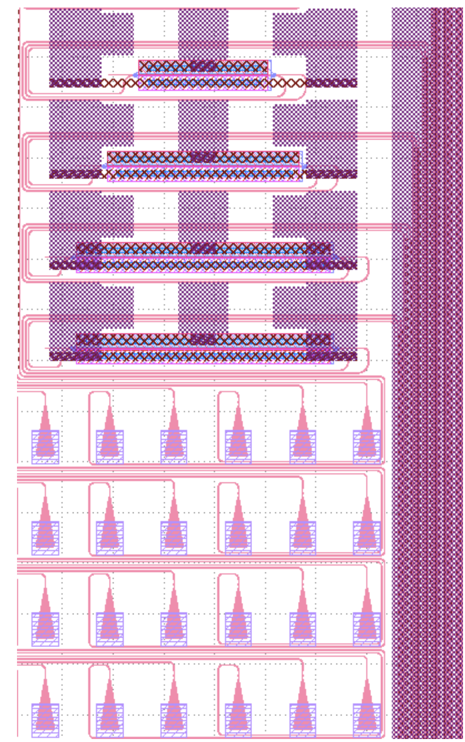


Workshop (summer)

Design & Modelling

Students submit:
- Proposal
- Design doc

Mask Layout



Students submit:
- Draft GDS
- Final GDS

Fabrication (Foundry)

Test

Students submit:
- Final report

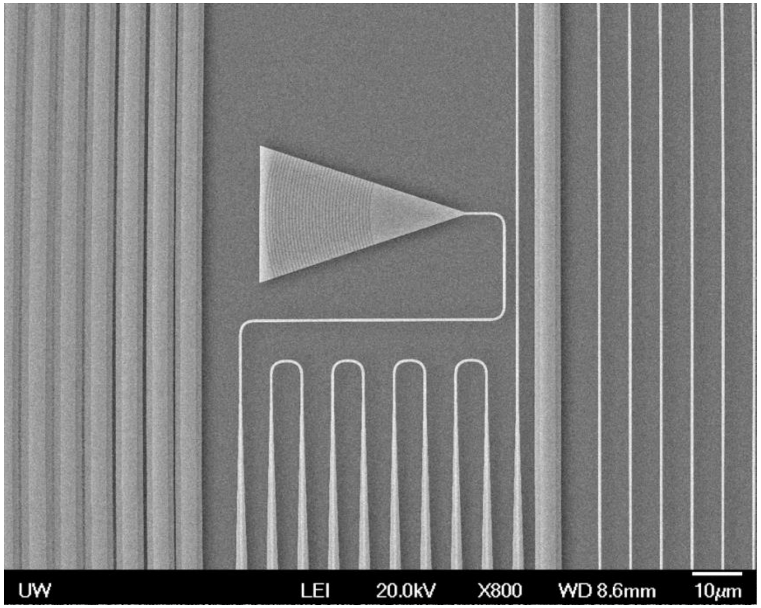
CMC MICROSYSTEMS

Silicon Electronic-Photonic Integrated Circuits (SiEPIC) Workshops – www.siepic.ubc.ca

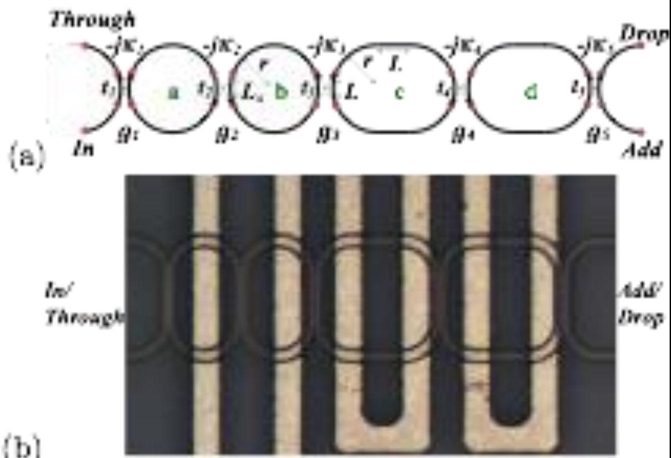
- Si-EPIC program – 4 annual workshops in:
  - **Passive Photonics – May 2014 at Laval University**
    - Fibre grating couplers, resonators (rings, disks, waveguide Bragg gratings, photonic crystals), splitters (ybranches, directional couplers), optical filters; via imec
  - **Active Photonics** (modulators and detectors) –
    - PN/PIN junction ring and Mach-Zehnder modulators, detectors; via CMC–IME
  - **CMOS Electronics for silicon photonics – August (?) 2014 at UBC**
    - modulator drivers, amplifiers for detectors, optical link analysis; via IBM
  - **Systems, Integration, Packaging – July 2014, McGill**
    - CMOS+photonic integration, system-level design and modelling, packaging
- Workshops open to all
  - Industry and academia (20 universities so far)

EBeam lithography

- Mature and established process at University of Washington.
- Costs:
  - as low as $1000 for a single-layer single-etch process 25x25 mm chip
  - to over $5000 per chip for a 3-etch chip with oxide cladding and dicing
- We have run several “MPW” chips
  - mimic the IME passives & ePIXfab imec passives, prior to sending to foundry
  - e.g., 1853 devices from 19 designers from 5 universities (~$2 per device)
    - automated testing for all devices (1 min per)



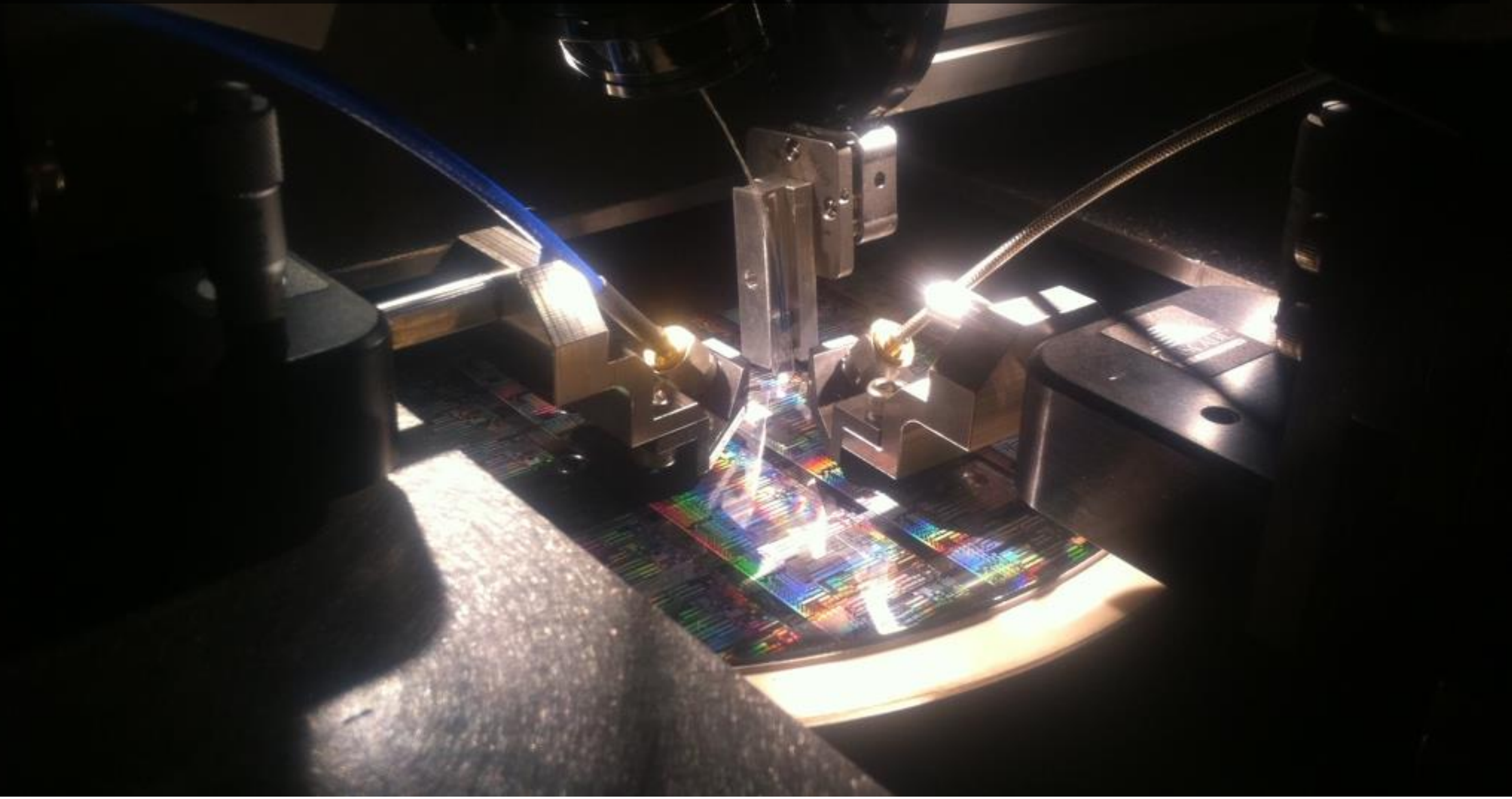
Robert Boeck, et al, *IEEE Photonics Journal*, 2013



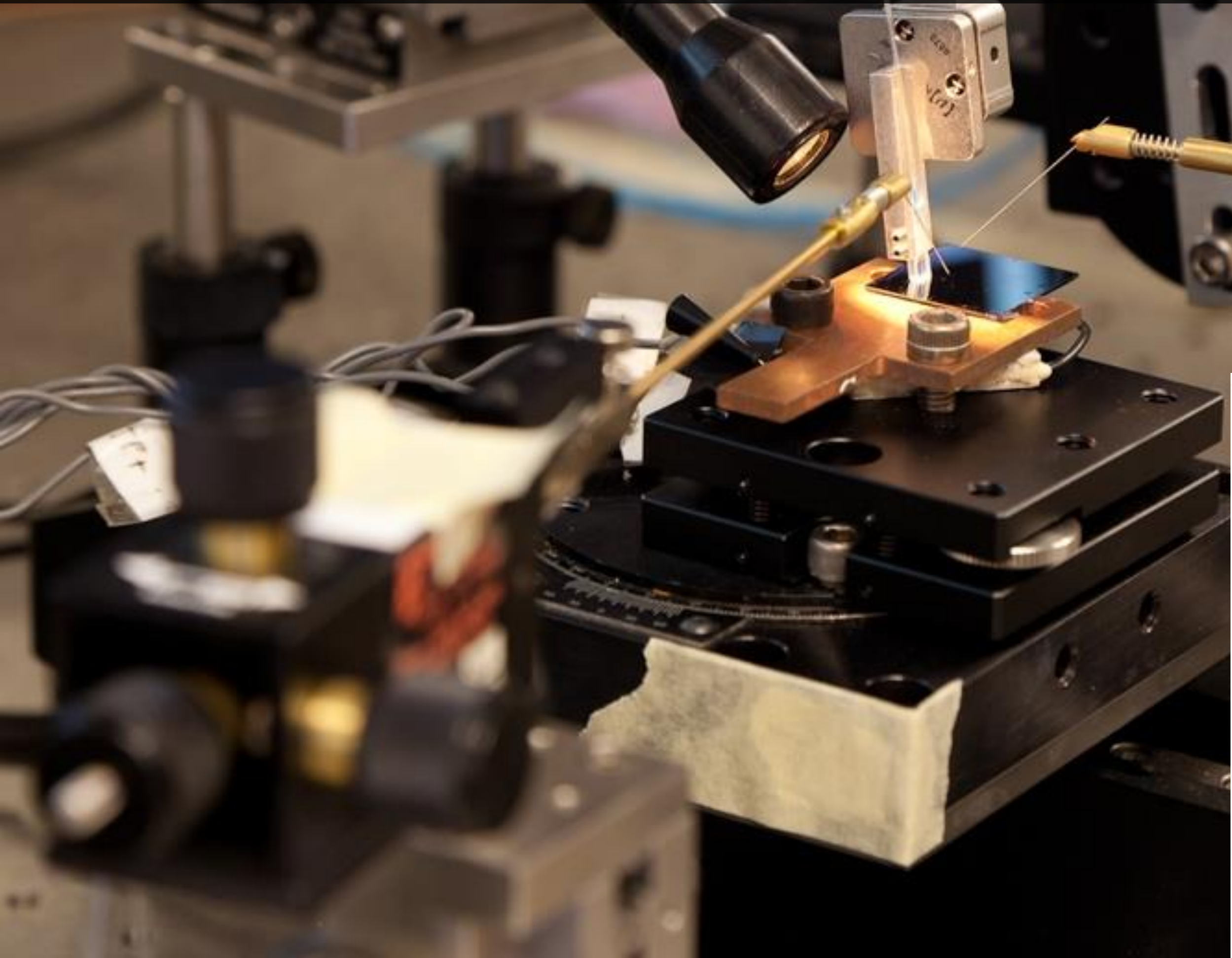
Robert Boeck, et al, *Optics Letters*, 07/2013

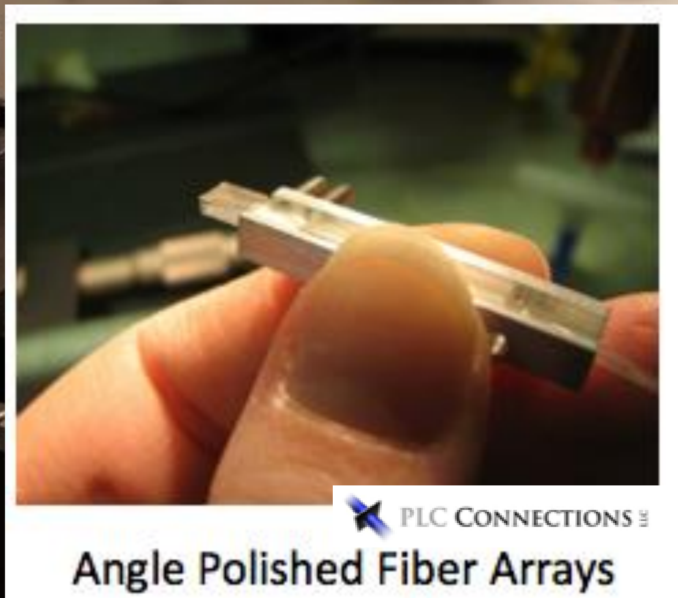
OpSIS Wafer-scale, normal incidence opto-electronic test setup:

- **Automated device navigation and optical alignment**
- **Manual electrical probing**

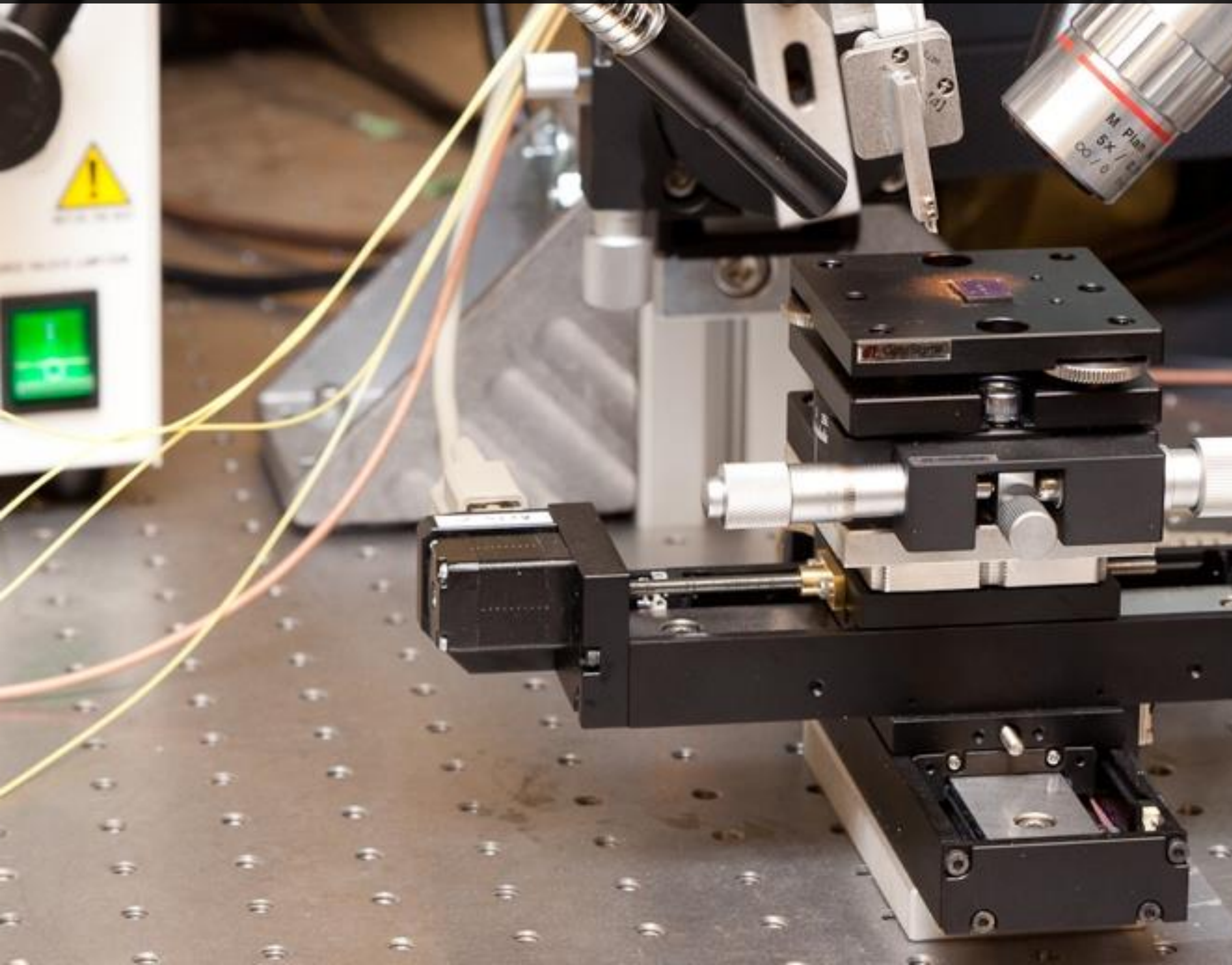


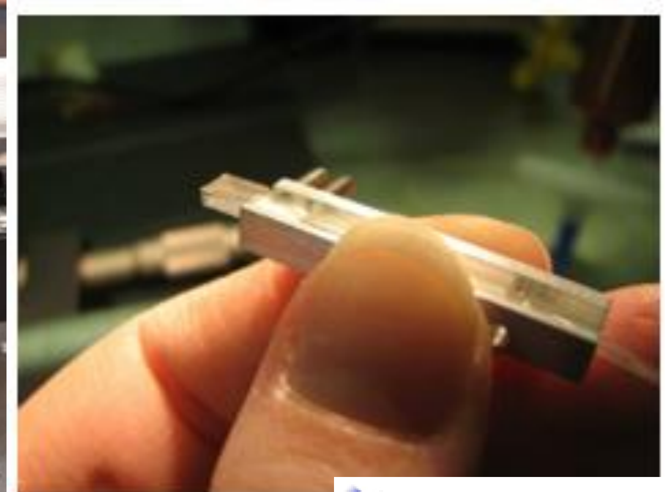
- Automated die-level test, for end-user:
  - – 30s per device (50,000 pts optical spectrum)
  - – Parts list ~ $20,000
    - (including nano-steppers, fibre array, microscope, except lasers)
  - – Software in Matlab – plans to “Open Source”





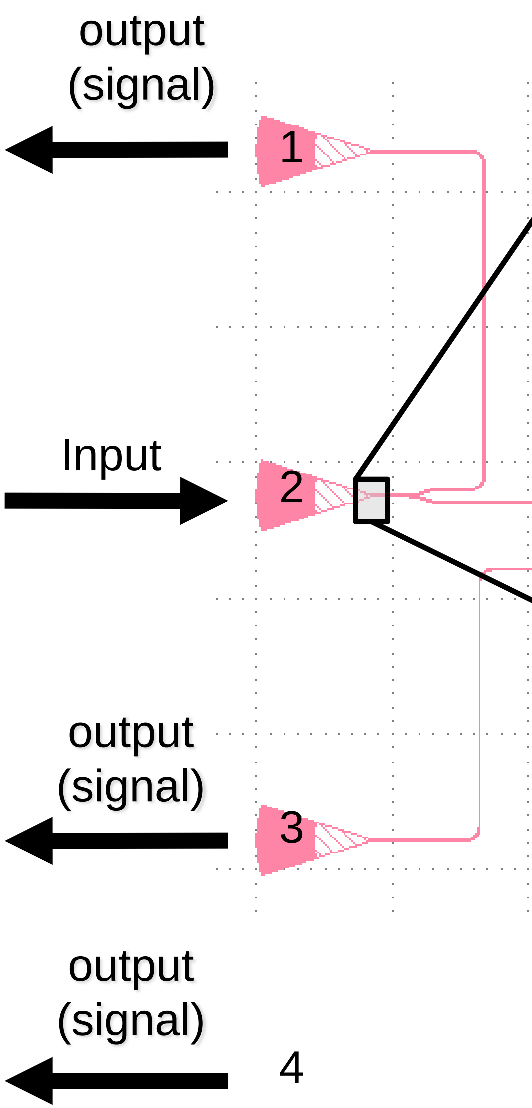
- Automated die-level test for end-user:
  - – 30s per device (50,000 pts optical spectrum)
  - – Parts list ~ $20,000
    - (including nano-steppers, fibre array, microscope, except lasers)
  - – Software in Matlab – plans to “Open Source”

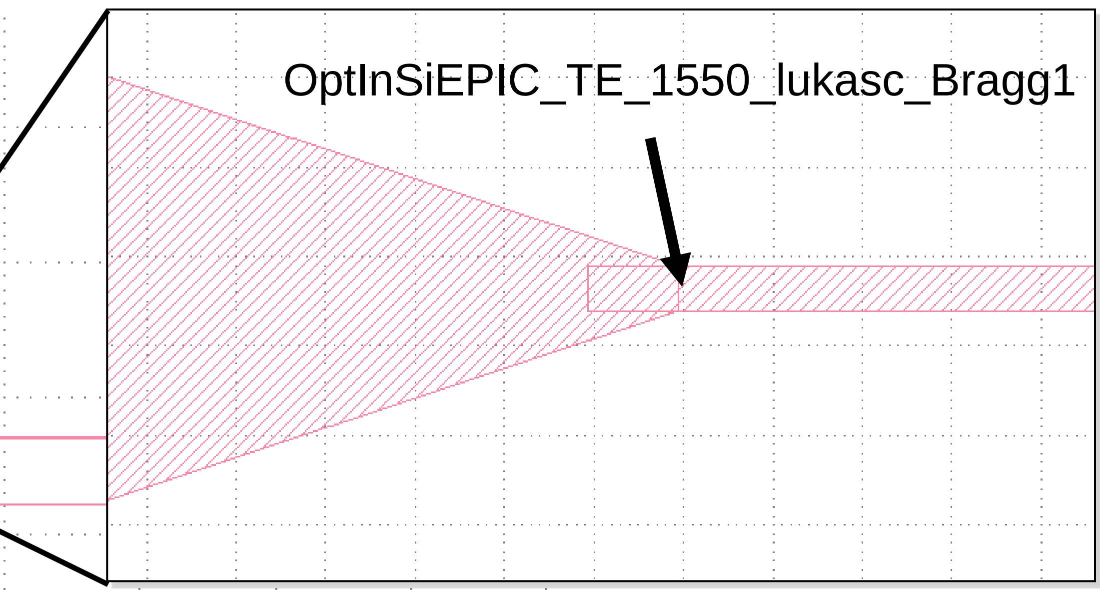




Angle Polished Fiber Arrays

Automated measurements – Locating devices





- Designer includes GDS "TEXT" labels on INPUT port of all devices (GC 2)
- Detectors connected to GC1, GC3, GC4, …
- Fine-align performed using GC1 and GC3
- 127 µm pitch

Why automated measurements?

- Parameter sweeps for process design kit (PDK) / Library development (grating couplers, optical resonators, 2x2 splitters):
  - Qiuhang Zhong, Wei Shi, Yun Wang, Lukas Chrostowski, David V. Plant, "**An Ultra-Broadband Fiber Grating Coupler with Focusing Curved Subwavelength Structures**", *Optical Fiber Communication Conference*, pp. Th2A.15, 03/2014
  - Han Yun, Wei Shi, Yun Wang, Lukas Chrostowski, Nicolas A. F. Jaeger, "**2 × 2 Adiabatic 3-dB Coupler on Silicon-on-Insulator Rib Waveguides**", *Proc. SPIE, Photonics North 2013*, vol. 8915, pp. 89150V, 06/2013
- Manufacturing variability studies – e.g., 371 identical devices on one chip:
  - Lukas Chrostowski, Xu Wang, Jonas Flueckiger, Yichen Wu, Yun Wang, Sahba Talebi Fard, "**Impact of Fabrication Non-Uniformity on Chip-Scale Silicon Photonic Integrated Circuits**", *Optical Fiber Communication Conference*, pp. Th2A.37, 03/2014
- Biophotonics
  - Samantha M. Grist, Shon A. Schmidt, Jonas Flueckiger, Valentina Donzella, Wei Shi, Sahba Talebi Fard, James T. Kirk, Daniel M. Ratner, Karen C. Cheung, Lukas Chrostowski, "**Silicon photonic micro-disk resonators for label-free biosensing**", *Optics Express*, vol. 21, issue 7, pp. 7994–8006, 03/2013
- Undergraduate courses
  - UBC EECE 403 – thermally tuned Mach-Zehnder switch – 25 students, 10 devices each – measured multiple times during fabrication (after EBL, after SiO_2 cladding, after metalization)
  - UBC EECE 484 – Bragg grating cavities – 25 students X 20 devices
- MPW runs
  - typically 4,000 devices, with 20+ designers

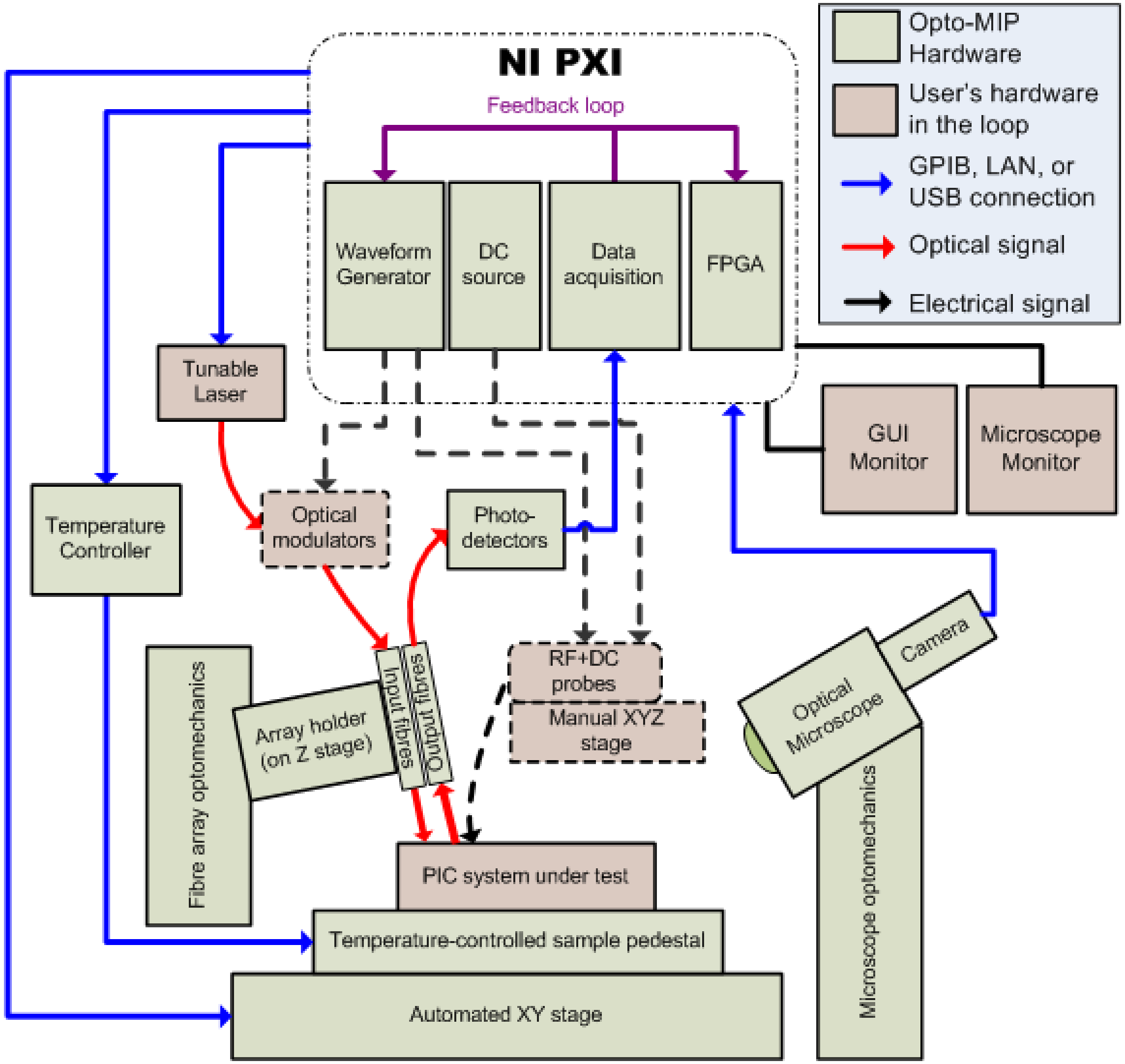
CMC Opto-MIP for Optical Gyroscopes

Miguel Á. Guillén-Torres, Maan Almarghalani,
Jonas Flueckiger, Lukas Chrostowski,
Nicolas A. F. Jaeger, Edmond Cretu

University of British Columbia

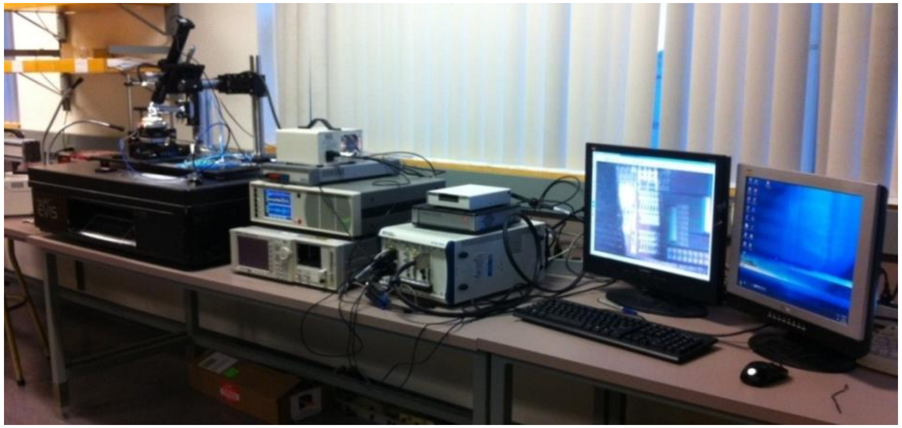
Silicon Photonics Microsystems Integration Platform

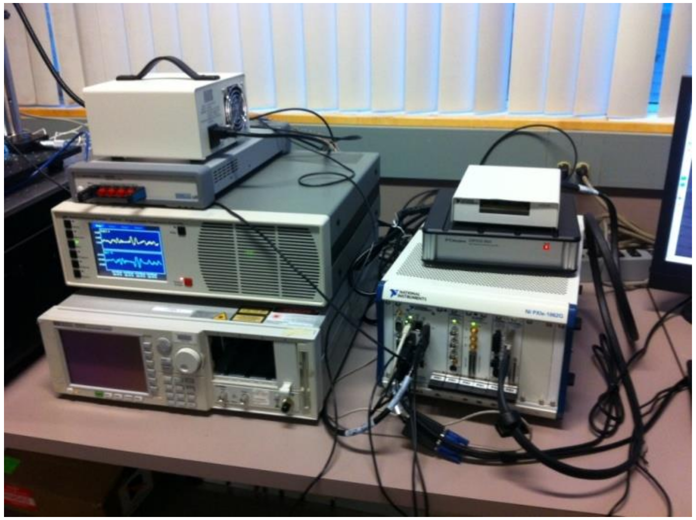
- System-level resources common with other MIP variants
- This project leverages such resources for testing Si Photonics integrated circuits (PICs)
- Automated opto-mechano-thermal systems characterization
- Modular design environment for multi-technology device validation
- Hardware-flexibility
- Optical, positioning and thermal instruments controlled via an NI-PXI



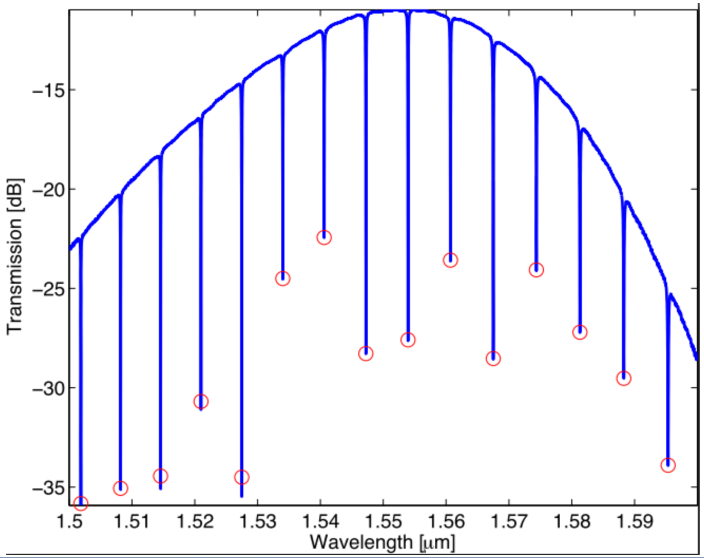
Multi-technology platform with configuration flexibility

- Benchtop configuration

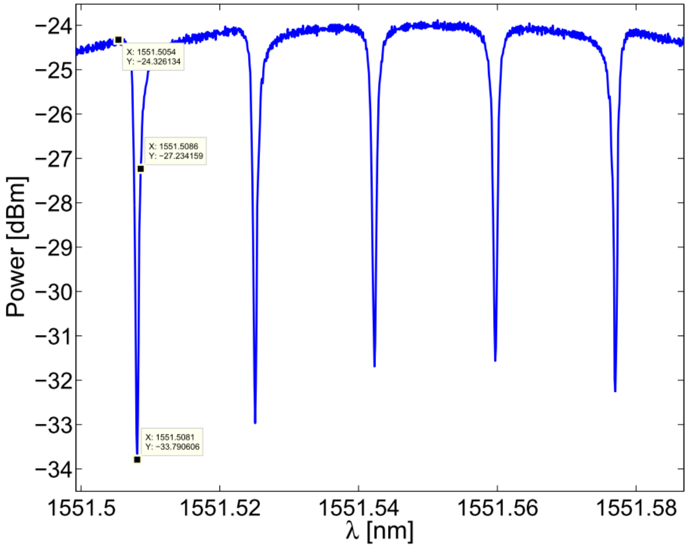




- Alignment Ring Spectra

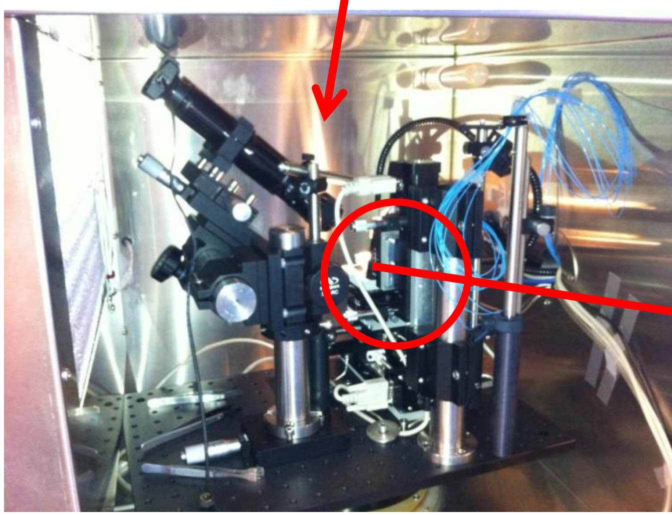


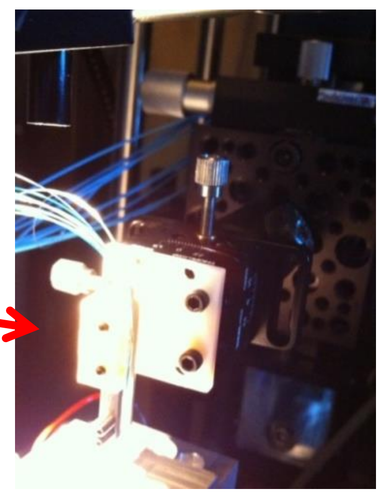
- Gyroscope rings, Q~ 1.5 M

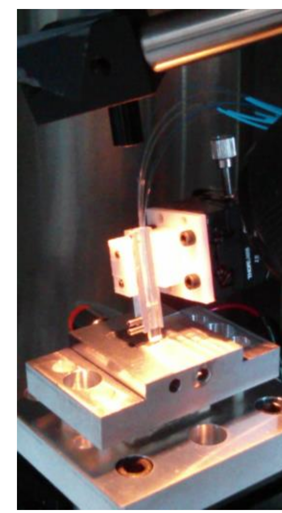


Compact setup configuration (small chamber)

- Based on successful prototyping at the benchtop level
  - Robust optomechanics for stable intertial, fluidic, or thermal Si-P system testing
- Shorter microscope
  - Enough space for electrical probing/fluidics
  - Manual positioning and focusing
- Fibre array holder
  - Manual pitch/roll/yaw goniometres/stages
  - Automated Z positioning
- Temperature-controlled vacuum chuck
  - Manual horizon adjustment
  - Automated XY positioning



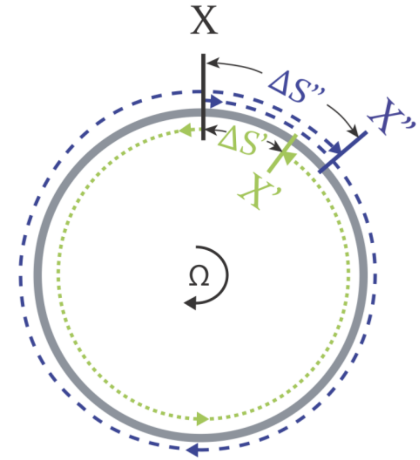




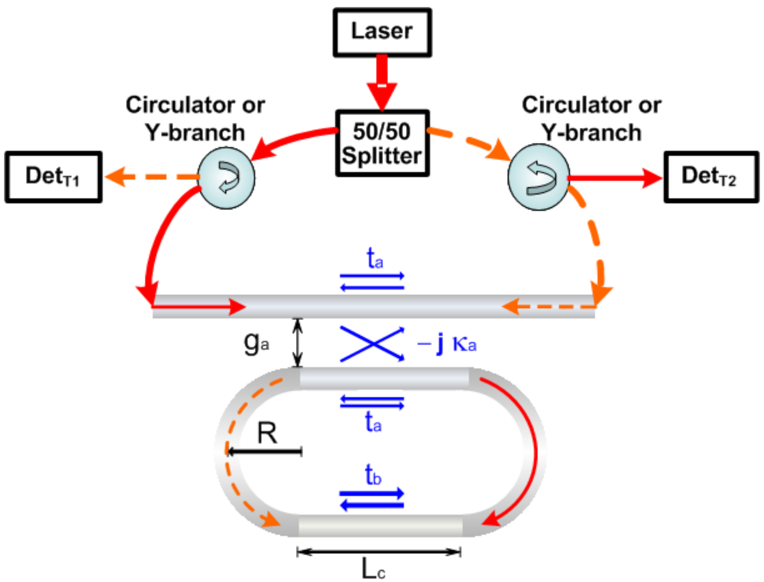
Specific application: Optical gyroscope validation

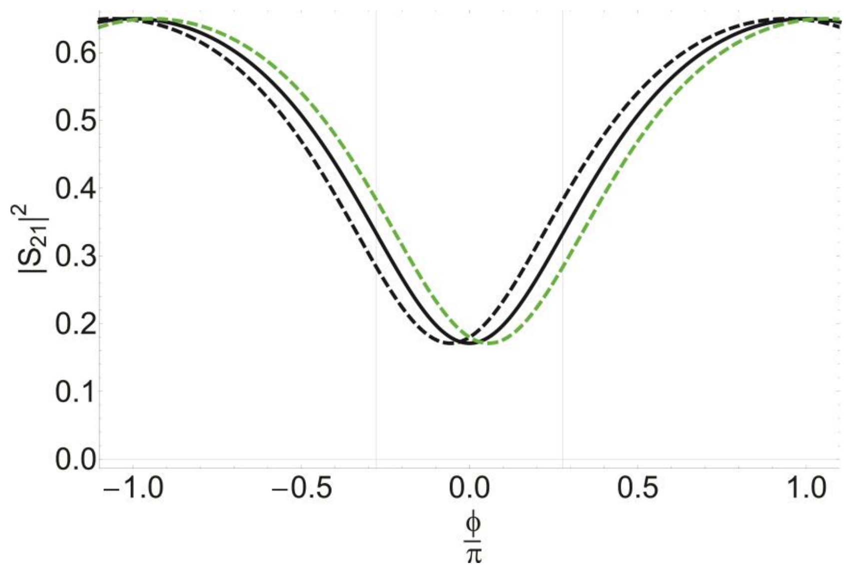
- Light travelling in a rotating medium is phase-shifted (Sagnac effect)
- Phase shift is proportional to the angular rate and the enclosed area Counter-propagating beams undergo opposite sign phase shifts
- Power variations enable angular speed sensing
- On-chip SOI gyroscope designs are tested using the Si-P MIP

$$\phi = \frac{2\pi n_{\text{eff}}(\lambda) L}{\lambda} \pm \frac{L^2 \Omega}{c\lambda_0}$$

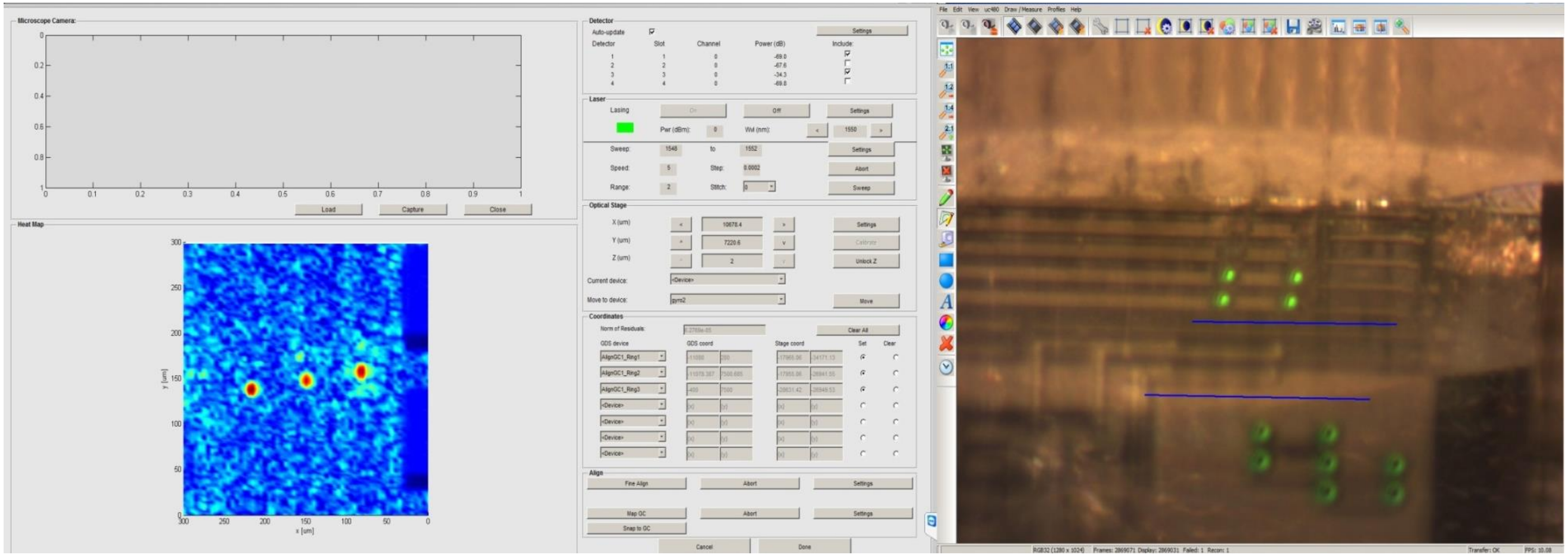


$$\Delta\phi = \frac{8\pi}{c\lambda_0}\vec{A}\cdot\vec{\Omega} = \frac{8\pi^2 R^2 \Omega}{c\lambda_0} = \frac{2L^2\Omega}{c\lambda_0}$$

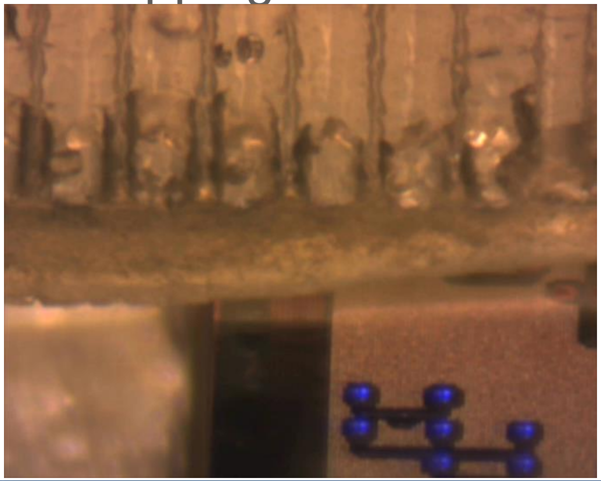




Fibre Array Positioning: Semi-Manual Control



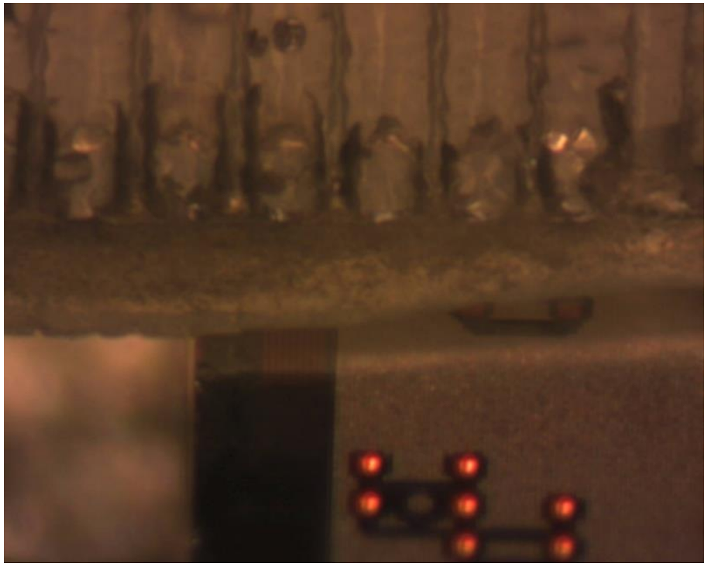
GC Mapping video:



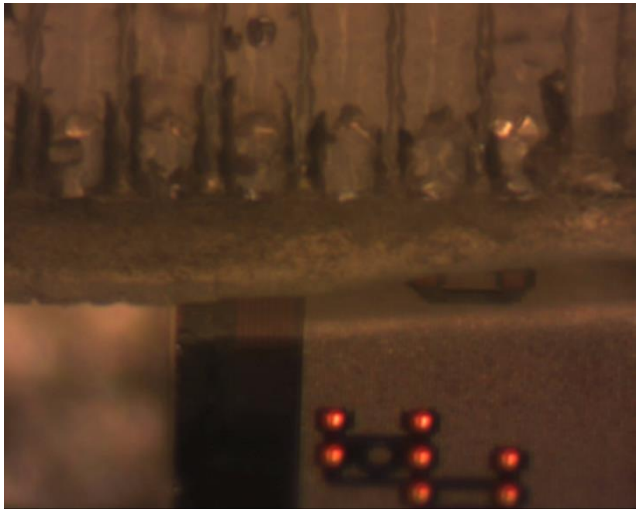
- Matlab GUI for manually control:
  - X, Y, and Z stage positioning
  - Laser and detector settings
- Raster scan function for coarse coupler mapping
- Suitable for fast single-device tests
- Used for coordinate mapping setup

Fibre array positioning (continued)

- Fine alignment sequences
  - Based on square-spiral and haircross gradient schemes
- Device coordinate mapping
  - Correlates device coordinates in a file to stage positions
  - Based on 3 device locations (preferably, at chip corners)
  - Generates device list for automated measurements
- Step 2: Automatic device tests
  - Automated, sequential device interrogation, using device list/map
  - Considerably faster than manual positioning and testing



GC Fine alignment video:



Compact Setup Results: Stability tests

– Pedestal temperature stability

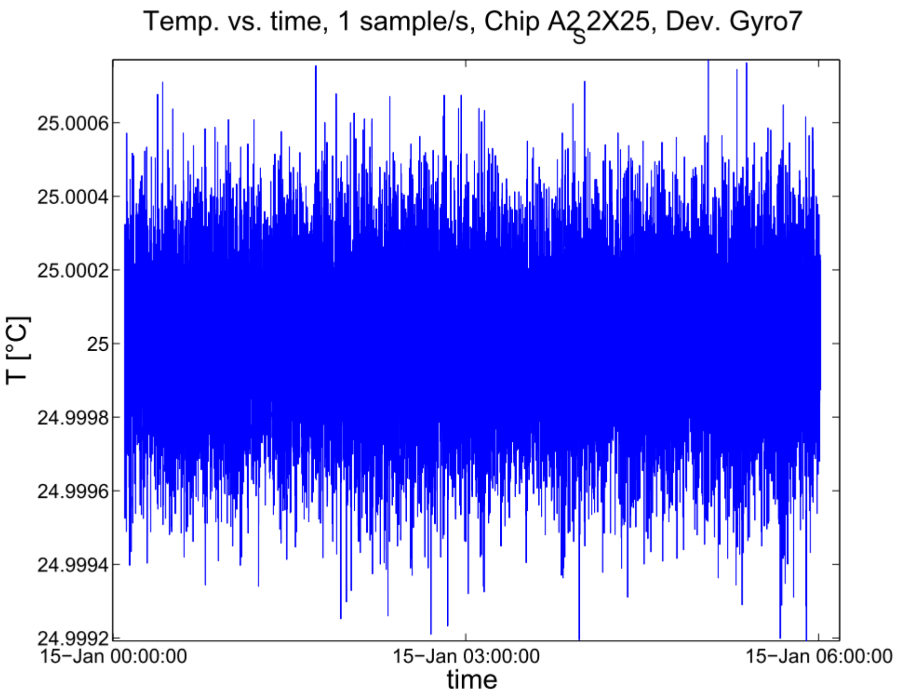
- ○ Capture time: 5.9 hours
- ✓ T_{avg} = 25 ^{o}C
- ✓ σ(T) = 0.2 mK

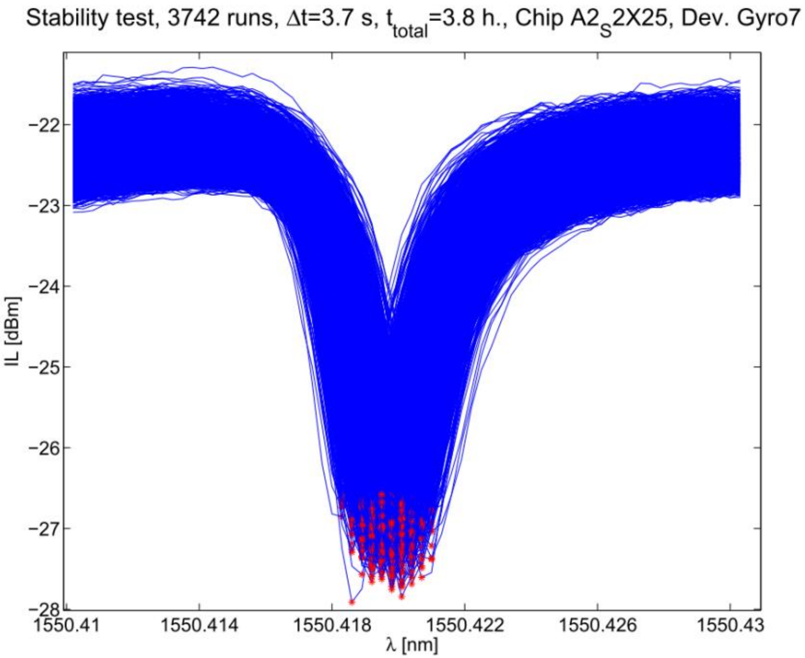
– Laser wavelength and power stability

Agilent 81682A specs:

- ▪ λ repeatability: ±1 pm
- ▪ λ stability: ± 1 pm
- ▪ P stability: ± 0.03 dB

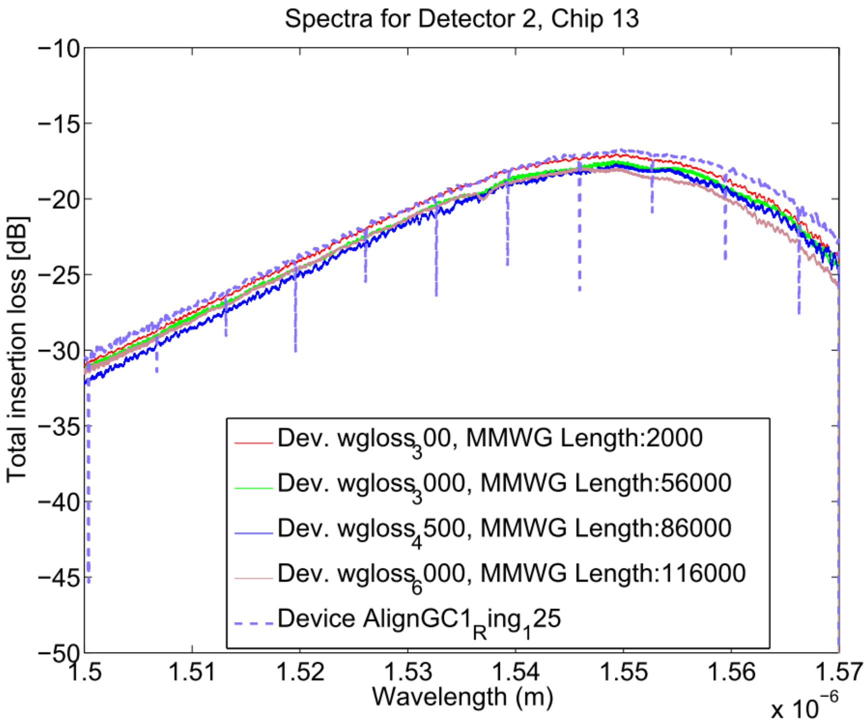
- ○ Sweep rate: 3.7 s
- ○ 3742 sweeps
- ○ Capture time: 3.8 h
- ✓ $\lambda_{0\ avg}$=1550.42 nm
- ✓ $\sigma(\lambda_0)$= 0.44 pm
- ✓ MaxDiff(λ_0)= 2.7 pm
- ➢ ΔP≈ 1.5 dB

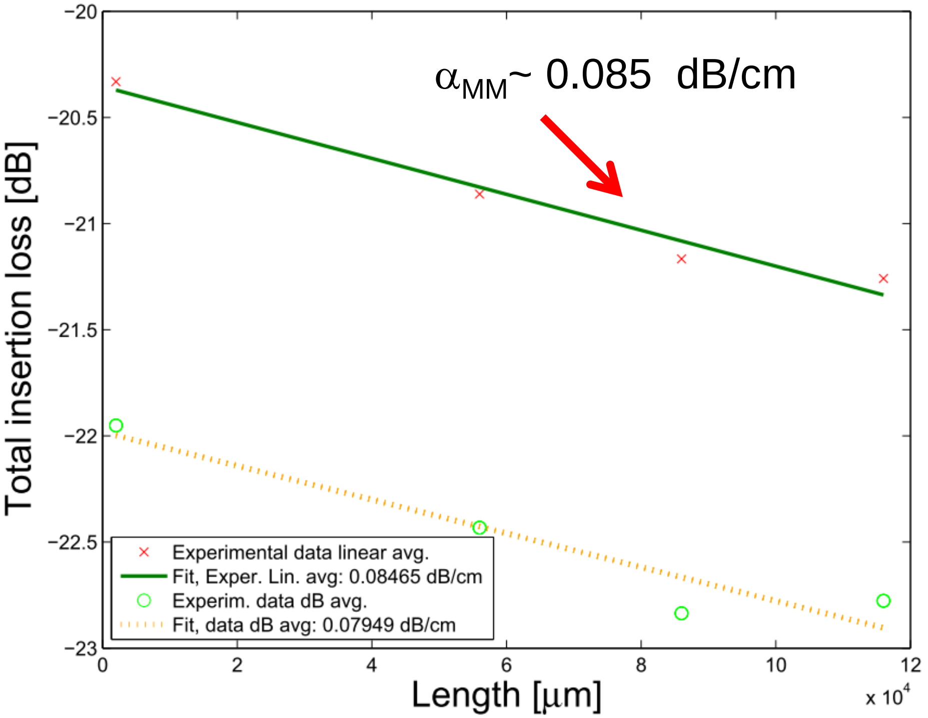




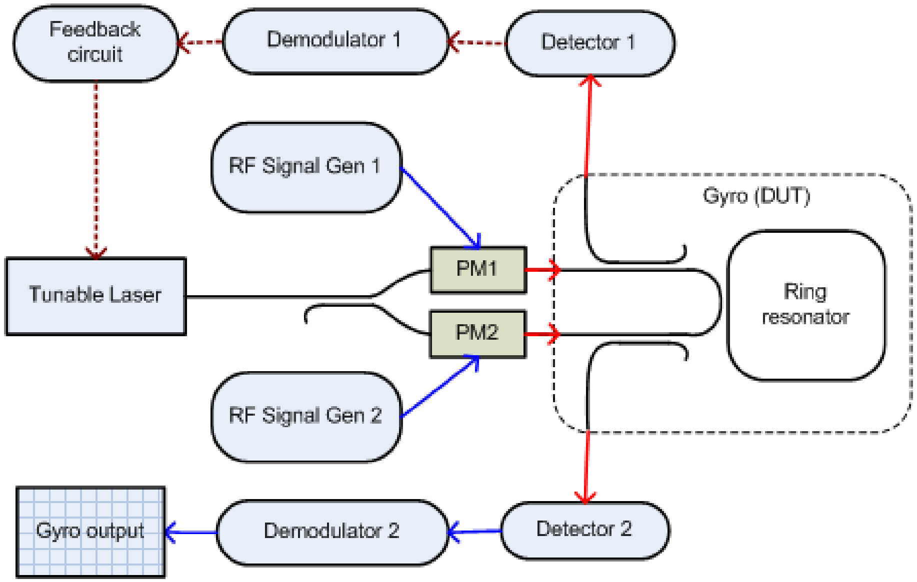
Compact Setup Results (cont’d): Propagation Loss

- Propagation loss test structures
  - Test structures with different SM or MM waveguide lengths
  - Spectral IL is measured in devices across the chip, several times
  - IL vs. Length fitting yields average propagation loss
- These waveguides allow for high Q resonators (1.5M)

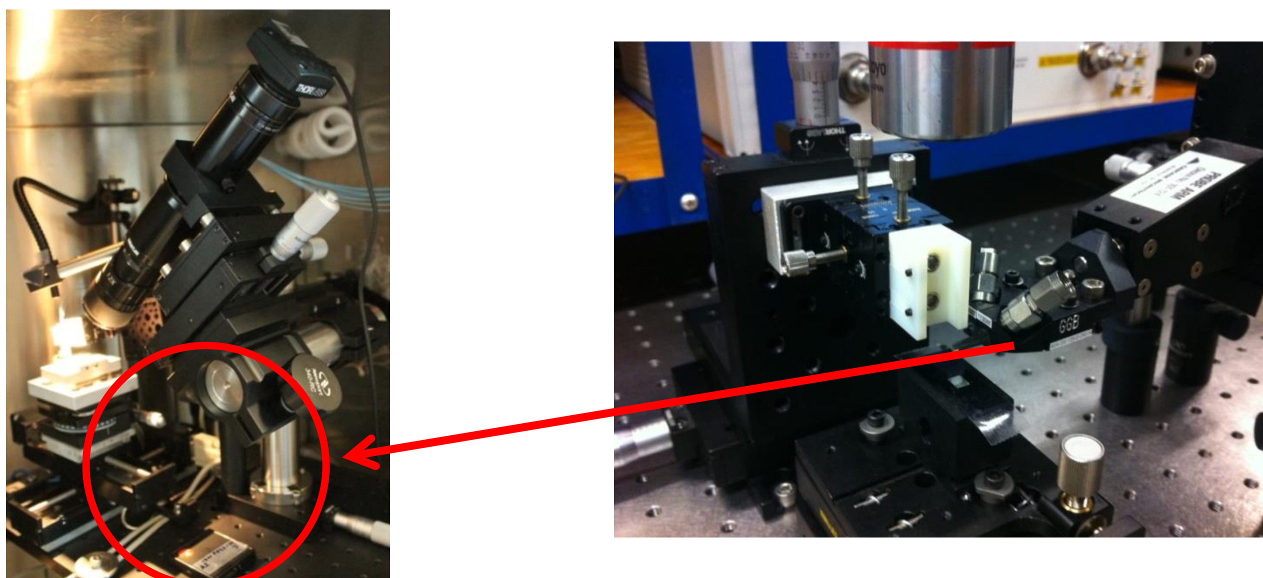




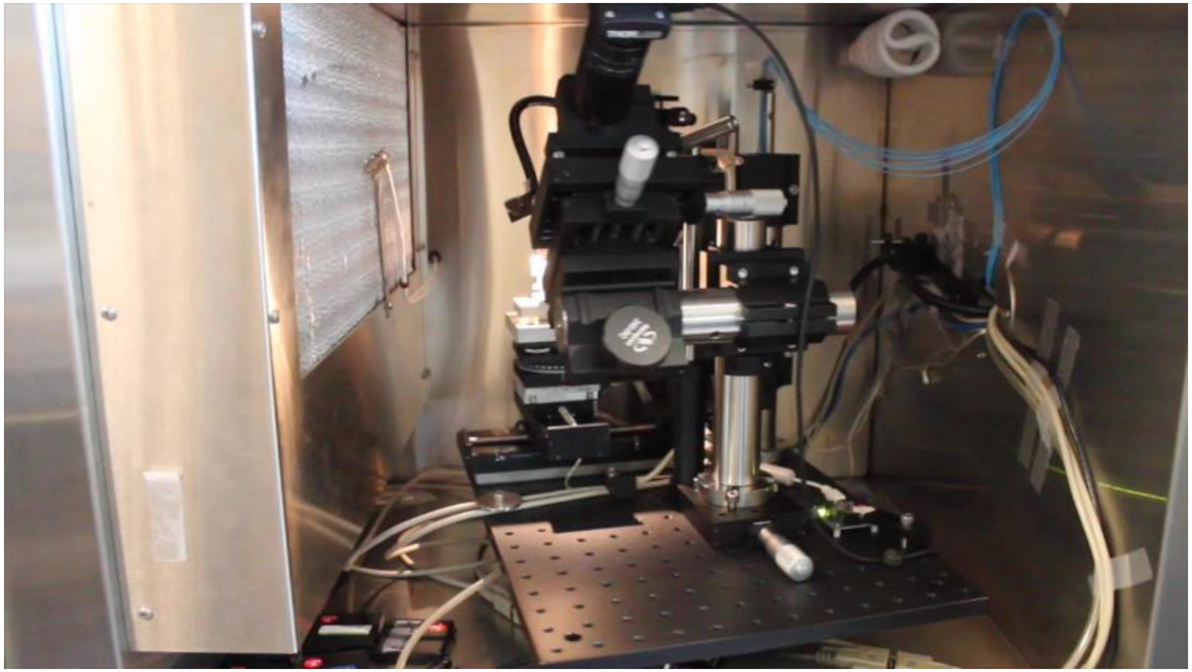
Gyroscope modulation scheme (under development)



- Area-efficient manual stages can be placed below the microscope
  - RF and DC chip probing
    - Advantages for gyroscope: Backscattering drift and noise effects reduction
- Steps towards smart fixtures in the field
  - Portable fixtures
  - Optical sources glued or integrated to the DUT



Rotational test video



MIP Resource Access

- MIP-related resources on CMC web site:

http://www.cmc.ca/WhatWeOffer/Prototyping/MIP.aspx

  - Reference design documents
  - User guides
  - Parts lists
  - Sample code

- Development systems community pages. Log in at:

https://community.cmc.ca/community/development-systems

How to access development systems through emSYSCAN

- There are currently ~25 MIPs installed in emSYSCAN member institutes across Canada.
  - The emSYSCAN project enables Canadian academic researchers to access these resources
- For information on how to access a development system:

http://www.cmc.ca/en/WhatWeOffer/Prototyping/AccessDevSys.aspx

emSYSCAN MIP Generation 2 Rollout

Generation 2 MIP rollout = approximately 25 systems to be delivered nationally, selected from 5-6 variants

Schedule for rollout:

- Institutes identify development system requirements from their institutional budgets (e.g. MIP vs SDR vs multi-core processor): May 2014
  - Involving researchers, local emSYSCAN coordinators, CMC
- If MIP identified, selection of MIP variant(s) for each institute: June-Aug 2014
- Purchase orders issued: Jan 2015
- Hardware delivery to institutes Apr 2015

MIP Variant Selection

List of host institute development system coordinators:

https://community.cmc.ca/docs/DOC-1515

Commercial ownership

- Managed on a case-by-case basis

What's next?

- MIP Generation 2 technical enhancements
  - Next CMC webinar is April 23
  - Providing descriptions and inviting feedback on Generation 2 of the MIP for 2015 emSYSCAN deliveries
  - MEMS, RF, microfluidic variants
  - http://www.cmc.ca/en/NewsAndEvents/Webinars/MIPGeneration2Webinar.aspx
- Smart fixture concept
  - Fixturing, packaging, reduced form factor control systems
  - Migrate your MIP prototype from the benchtop to the application environment
  - Towards higher TRL

We're interested in your feedback

CMC MICROSYSTEMS

- MIP for Si-photonic hardware-in-the-loop
  - Rob Mallard; mallard@cmc.ca
  - Miguel Torres, Lukas Chrostowski; miguela@ece.ubc.ca lukasc@ece.ubc.ca
- MIP hub and other variants
  - Susan Xu; xu@cmc.ca
- emSYSCAN development systems allocations
  - Hugh Pollitt-Smith; pollitt-smith@cmc.ca
- Interest in the Smart Fixture concept
  - James Millar; millar@cmc.ca