Keysight N4963A
Clock Synthesizer 13.5 GHz

User's Guide

KEYSIGHT TECHNOLOGIES

Notices

Manual Part Number

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For Assistance and Support

http://www.keysight.com/find/assist

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Safety Notices

CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

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NOTE

A **NOTE** provides important or special information.

Safety Summary

General Safety Precautions

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument.

Keysight Technologies assumes no liability for the customer's failure to comply with these requirements.

Before operation, review the instrument and manual for safety markings and instructions. You must follow these to ensure safe operation and to maintain the instrument in safe condition.

Initial Inspection

Inspect the shipping container for damage. If there is damage to the container or cushioning, keep them until you have checked the contents of the shipment for completeness and verified the instrument both mechanically and electrically. The Performance Tests give procedures for checking the operation of the instrument. If the contents are incomplete, mechanical damage or defect is apparent, or if an instrument does not pass the operator's checks, notify the nearest Keysight Technologies Sales/Service Office.

WARNING To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any portion of the outer enclosure (covers, panels, etc.).

General

This product is a Safety Class 1 product (provided with a protective earthing ground incorporated in the power cord). The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. Any interruption of the protective conductor, inside or outside of the instrument, will make the instrument dangerous. Intentional interruption is prohibited.

Environment Conditions

This instrument is intended for indoor use in an installation category II, pollution degree 2 environment per IEC 61010 Second Edition and 664 respectively. It is designed to operate within a temperature range of 10 to 40 °C at a maximum relative humidity of 80% for temperatures up to 31 °C, decreasing linearly to 50% relative humidity at 40 °C at an altitude of 2000 meters.

This module can be stored or shipped at temperatures between -40°C and +70°C. Protect the module from temperature extremes that may cause condensation within it.

Before Applying Power

Verify that all safety precautions are taken. The power cable inlet of the instrument serves as a device to disconnect from the mains in case of hazard. The instrument must be positioned so that the operator can easily access the power cable inlet. When the instrument is rack mounted the rack must be provided with an easily accessible mains switch.

Ground the Instrument

Install the instrument so that the ON / OFF switch is readily identifiable and is easily reached by the operator. The ON / OFF switch is the instrument disconnecting device. It disconnects the mains circuits from the mains supply before other parts of the instrument. Or the detachable power cord can be removed from the electrical supply. Alternately, an externally installed switch or circuit breaker which is readily identifiable and is easily reached by the operator may be used as a disconnecting device.

Do Not Operate in an Explosive Atmosphere

Do not operate the instrument in the presence of flammable gases or fumes.

Do Not Remove the Instrument Cover

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made only by qualified personnel.

Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

Symbols on Instruments

The instruction documentation symbol. The product is marked with this symbol when it is necessary for the user to refer to the instruction in the documentation.

C-Tick Conformity Mark of the Australian ACA for EMC compliance.

ICES/NMB-001

This mark indicates compliance with the Canadian EMC regulations.

ISM 1-A

This text denotes the instrument is an Industrial Scientific and Medical Group 1 Class A product.

CE Marking to state compliance within the European Community: This product is in conformity with the relevant European Directives. EMC Directive 2004/108/EC and Low Voltage Directive 2006/95/EC.

This symbol indicates that internal circuits can be damaged by electrostatic discharge (ESD), therefore, avoid applying static discharges to the panel input connectors.

China RoHS regulations include requirements related to packaging, and require compliance to China standard GB18455-2001 or, for paper / fibreboard packaging an internationally recognized marking such as ISO standard symbol is acceptable. Keysight will comply with China RoHS packaging marking requirements by implementing the ISO standard recycling symbol marking on all primary (generally for customers) and secondary (generally for distributors) fibreboard packaging for goods covered by China RoHS. Tertiary packaging (generally for shippers, i.e. shrink wrapping and pallets) are not required to be marked. At this time Keysight will not be marking solid wood packaging.

Indicates the time period during which no hazardous or toxic substance elements are expected to leak or deteriorate during normal use. Forty years is the expected useful life of the product.

The Korean Certification (KC) mark is required for products that are subject to legally compulsory certification.

The KC mark includes the marking's identifier code that has up to 26 digits and follows this format: KCC-VWX-YYY-ZZZZZZZZZZZZ.

This symbol indicates that the instrument requires alternating current (AC) input.

This symbol indicates that the power line switch is in the ON position.

This symbol indicates that the power line switch is in the OFF position.

General Recycling Mark

Environmental Information

This product complies with the WEEE Directive (2002/96/EC) marketing requirements. The affixed label indicates that you must not discard this electrical/electronic product in domestic household waste.

Product category: With reference to the equipment types in the WEEE Directive Annexure I, this product is classed as a "Monitoring and Control instrumentation" product.

Do not dispose in domestic household waste.

To return unwanted products, contact your local Keysight office, or see

www.keysight.com/environment/product/ *for more information.*

Contents

1 Getting Started

1.1 General

The N4963A Clock Synthesizer 13.5 GHz generates six pairs of differential square-wave clock outputs from 500 MHz to 13.5 GHz. The instrument features GPIB-programmable output amplitude, DC offset, phase offset, sub-rate trigger, and jitter injection.

The N4963A feature set includes:

- Clock generation from 0.5 to 13.5 GHz
- GPIB-adjustable output parameters
- 1 Hz to 100 MHz jitter injection (N4963A-101)

Applications

- Multi-lane PRBS eye-mask testing
- Multi-channel stressed eye BER testing
- Crosstalk analysis with multiple aggressors
- General instrument-grade clock generation

Key Features

- Low cost, high performance
  - Intrinsic jitter <2 pS
  - Rise/fall times <40 pS
- Six differential clock outputs
  - Two differential front panel outputs (jittered and reference)
  - Four differential rear panel outputs (two jittered and two reference)
- GPIB programmable output parameters
  - Output amplitude: 1.2 - 4 V pp diff.
  - DC offset voltage: -2 V to +2 V
  - Phase offset: 360-degrees (1 UI)
- Designed for testing datacom standards
  - Operates 0.5 to 13.5 GHz
  - High-UI jitter injection (N4963A-101)

Internal clock system

- Internal or external 10 MHz reference
- Synthesized 0.5 to 13.5 GHz clock
- Programmable low-rate trigger output (divide-by-8,9,10,...,510,511)

Reference Output Phase Offset	• 36o degree (1 UI) programmable offset • 2 degree minimum step size
Output Amplitude	• Front panel, single-ended 0.6 to 2 V pp • Rear panel, single-ended 0.2 to 0.8 V pp • Front panel, DC offset -2 V to +2 V
Display	• LED indicators and display
Interface	• Local push-button control • GPIB (IEEE 488.2-1992) • All controls both local and GPIB
Jitter Generation (N4963A-101)	• Internal jitter synthesizer: o 1 Hz to 75 kHz Max 32 UI o 75 kHz to 2.4 MHz Max 32 -> 1UI o 2.4 MHz to 100 MHz Max 0.6 UI • Also features external jitter input

1.2 Getting started with N4963A

1.2.1 Unpacking and installation

The N4963A clock synthesizer 13.5 GHz is shipped in a protective carrying case with all the accessories required for the self-test mode and verification. The case includes:

- N4963A clock Synthesizer
- AC power converter module
- AC power cord
- CD containing the N4963A user guide and N4963A data sheet

WARNING **If this product is not used as specified, the protection provided by the equipment could be impaired. This product must be used in a normal condition (in which all means for protection are intact) only.**

CAUTION Before switching on this instrument, make sure the supply voltage is in the specified range.

CAUTION This instrument has auto ranging line voltage input. Be sure the supply voltage is within the specified range.

In an ESD-safe environment, carefully remove the N4963A from the case. Install on a flat surface with unobstructed air flow to the back panel. Plug the AC power cord into the power converter module and a wall socket, then plug the converter module into the N4963A.

1.2.2 Important notes

- Use ESD protection at all times when using the instrument
- Review min/max specifications before applying input signals
- Use only SMA-connectors on the RF ports
- Use only BNC-connectors on the 10MHz reference ports
- Use dust jackets on unused back panel connectors
- Situate the instrument away from heat sources, do not block the fan

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1.2.3 Performance recommendations

1. When using differential-mode connections, ensure the cables are phase balanced
2. Differential connectors may be used single-ended if second end terminated in 50 Ω
3. Use high quality cables and connector savers (or adaptors)
4. Keep cable lengths short and minimize number of cable bends
5. Use a 7 to 10 in-lbs torque wrench when attaching connectors

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1.3 Connect The Hardware

- Connect power cord to adaptor to N4963A; plug in the power cord.
- Connect the *Jittered* **OUT** to your instrument transmit clock input using the filters provided. Note: Filters are provided for 6-11.5 GHz and 9-13 GHz operation.
- Connect the *Reference* **OUT** to your instrument receive clock input using the filters provided. Note: Filters are provided for 6-11.5 GHz and 9-13 GHz operation.
- Connect the **Trig-O** to the trigger input of your sampling instrument (the default trigger output frequency is clock frequency/8).
- If using an external reference, connect the reference to the **10 MHZ IN** BNC connector.

1.4 Setting frequency and output levels

- Turn on the power switch from the back panel.
- The N4963A synthesizer starts with the **FREQ** option selected by default and "005.000G" showing in the display.
- Set the desired frequency using the **Unit, Digit** and **Value** buttons.
- Press the *Display*->**Scroll** ↓ button and select **AMP.** Select the output channel bank with the **Chan** button. Set the desired single-ended peak-to-peak voltage using the **Unit, Digit** and **Value** buttons.
- Press the *Display*->**Scroll** ↓ button and select **DC OFFSET**. Select the output channel bank with the **Chan** button. Set the desired DC offset voltage using the **Digit** and **Value** buttons.
- If using an external reference, press the **Ext 10MHz** button, and the indicator will light. The internal reference is being used if the indicator is off.
- To turn on the clock output and the trigger signal, press the *Clock*->**On** button. The green LED will light indicating the synthesizer is transmitting.

1.5 Aligning clock and data

- The front panel *Reference Output* (channel 1) signal can be phase shifted relative to all other output channels.
- Press the *Displa*->**Scroll** ↓ button and select **DELAY**. Set the phase offset between channel 1 and all other channels using the **Digit** and **Value** buttons.
- Center the reference clock for minimum BER or other desired state.

1.6 Enabling jitter injection

- Using the jitter **Select** button, select either the internal (**Int Jitter**) or external (**Ext Jitter**) jitter source.
- Using the internally generated jitter source (**Int Jitter**):
  - Press the *Display*->**Scroll** ↓ button and select **JITTER FREQ**.
  - Set the modulation frequency with the **Unit, Digit** and **Value** buttons.
  - Press the *Display*->**Scroll** ↓ button until the **MORE** indicator LED is lit and the display shows "J xx.x ui". Adjust the amount of jitter using the **Value** button.
- Using an external source for phase jittering (**Ext Jitter**):
  - Press the *Display* ->**Scroll** ↓ button and select **JITTER FREQ**.
  - **JITTER FREQ** indicates low jitter frequency mode, "Ext LO", or high jitter frequency mode, "*Ext HI*". Toggle with the **Value** button.
  - "*Ext LO*" mode should be used for modulation frequencies below 2.4 MHz. The input is digitally sampled and the amount of jitter can be scaled by pressing the *Display*->**Scroll** ↓ button until the display shows "*ExtUI*=xx". Use the **Value** button to set the scaling factor ("*ExtUI*=16" sets the scale of 16 UI for 1Vpp input amplitude).
  - "*Ext HI*" mode should be used for modulation frequencies above 2.4MHz. The amount of jitter injected is directly related to the amplitude of the applied signal, to a maximum extent of 0.6 UI.

2 N4963A Operation Overview

The Keysight Technologies N4963A clock synthesizer 13.5 GHz generates six pairs of differential square-wave clock outputs from 500 MHz to 13.5 GHz. The instrument features GPIB-programmable output amplitude, DC offset, phase offset, sub-rate trigger, and jitter injection.

Figure 1 illustrates a typical output, as measured on a Keysight 86100 DCA. Shown is the 2 GHz output from the front-panel reference (blue) and jittered (red) clock outputs. The jitter is applied internally at 100 kHz, 0.3 UI is injected in this case.

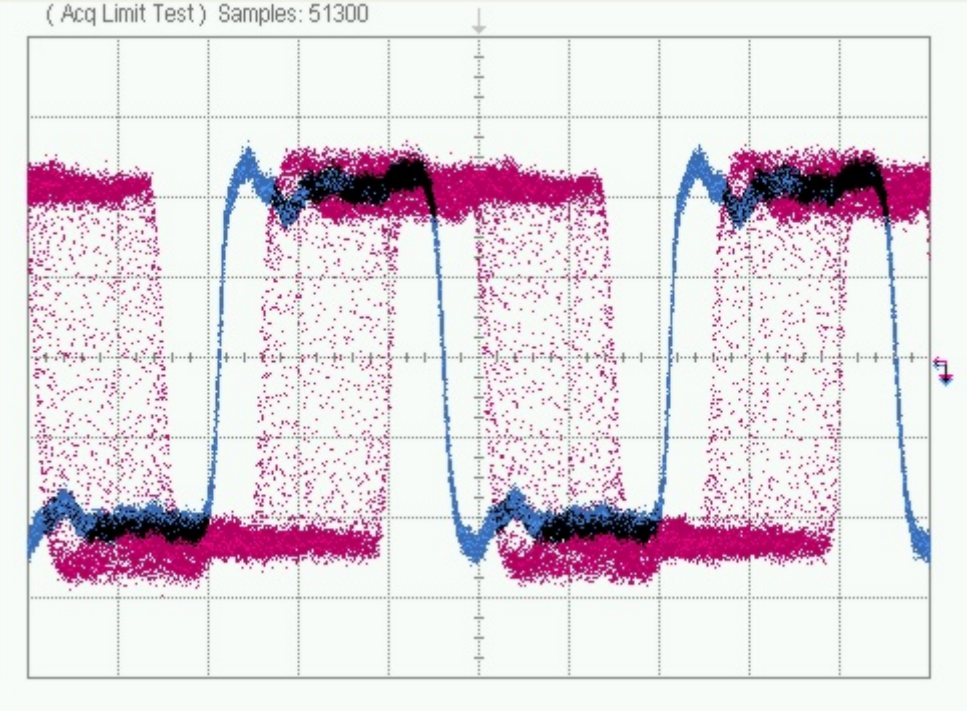

Figure 1. 2 GHz reference (blue) and 0.3UI @ 100 kHz jittered (red) clock outputs

3 N4963A System Overview

Control

System configuration settings are all available from the local push-button interface or remote GPIB (IEEE 488.2) interface. Instrument status is conveyed on the front panel by LED indicator and the 8-digit display.

Options

The N4963A is available with the following build options:

- standard: 500 MHz to 13.5 GHz operation, 6 differential unjittered outputs
- N4963A-101: Adds jitter injection capability to 3 differential output channels

Block Diagram

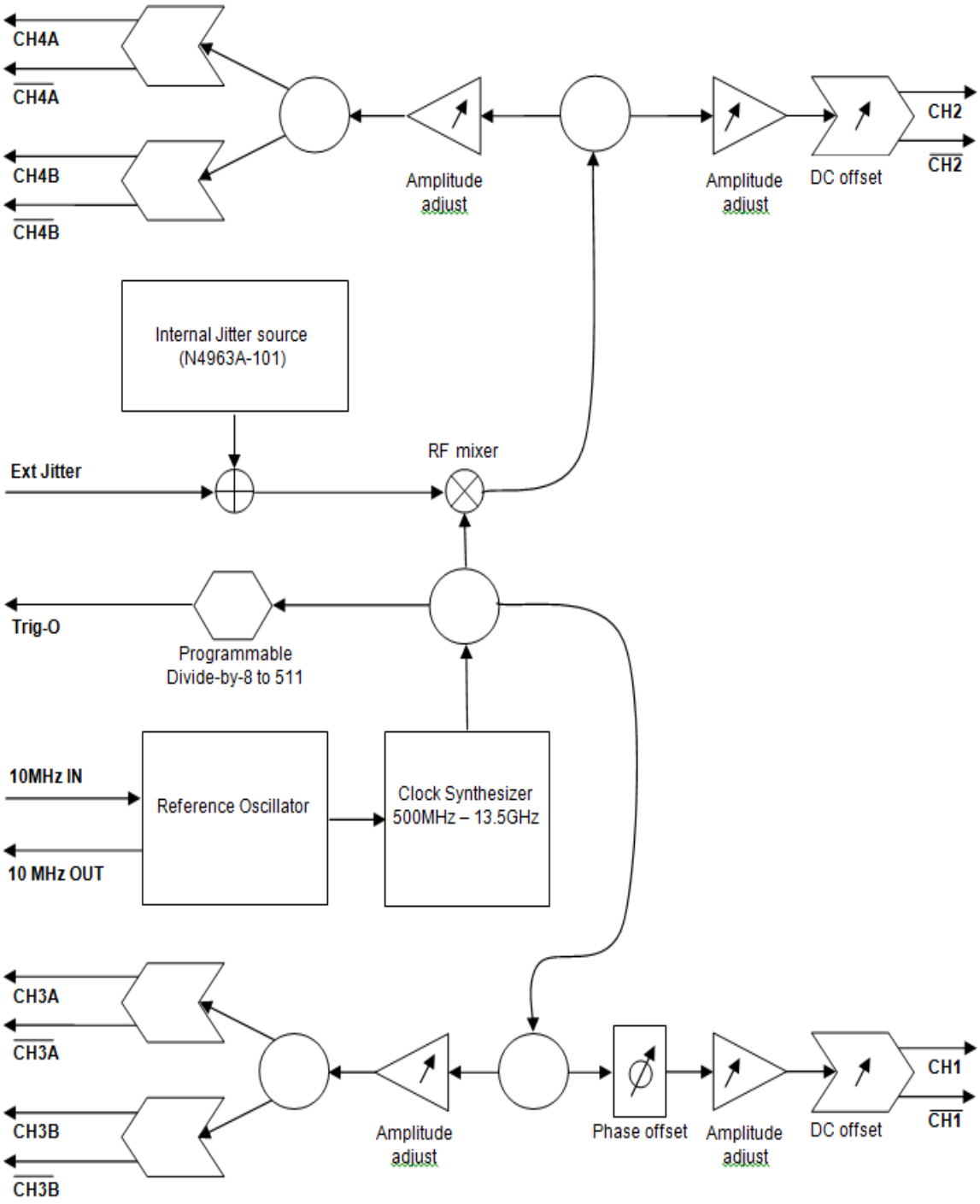

Figure 2. N4963A block diagram

3.1 Front panel quick reference

Figure 3. N4963A front panel

3.1.1 Connectors

Reference Outputs: OUT, $\overline{\text{OUT}}$ (SMA) – differential unjittered outputs, channel 1

Jittered Outputs: OUT, $\overline{\text{OUT}}$ (SMA) – differential jittered outputs, channel 2

3.1.2 Front panel controls

Table 1. Front panel control and indicator details

Label	LED indication	Button Function
Local	On- Local control Off- GPIB control	Switches unit control from GPIB to front panel control.
Clock	On- System on Off- System off	Turns clock and trigger outputs on and off.

Label	LED indication	Button Function
Ext 10 MHz	On- External ref Off- Internal ref	Toggles the 10 MHz reference clock between an externally-applied source and the internally-generated source.
Select (Jitter): Jitter Off Int Jit Ext Jit	Off- All jitter off Int- Internal jitter Ext- External jitter	Requires N4963A-101. Toggles between injecting no jitter, injecting jitter from the internal jitter generator, and injecting jitter from the externally-applied source.
Chan +/-		Selects output channel for parameter change. Amplitude channels A1 (front reference), A2 (front jittered), A3 (back), A4 (back). DC offset channels O1 (front reference), O2 (front jittered).
Value +/-		Increases or decreases the currently displayed parameter value.
Digit +/-		Selects the digit of the currently displayed parameter. Selected digit blinks on display.
Unit +/-		Selects the unit of the currently displayed parameter value. Options are G (GHz), M (MHz), and K (kHz).
Scroll		Selects the menu option to display and modify.
FREQ	Clock frequency	
AMP	Output amplitude	
DC OFFSET	Output DC offset	
DELAY	Phase offset	
JITTER FREQ	Jitter frequency	
MORE	Other menu option	
Unleveled	On- Unleveled	Turns on if any of the output amplitudes become un-calibrated.

The default power-on settings are listed in Table 12 on page 44.
The front-panel controls are further discussed in Section 5.2.

3.2 Rear panel quick reference

Figure 4. N4963A rear panel

3.2.1 Connectors

10 MHz IN, 10 MHz OUT (BNC) – 10 MHz reference input and output

Jit CH4A, $\overline{\text{CH4A}}$ (SMA) – Differential jittered outputs, channel 4

Ref CH3A, $\overline{\text{CH3A}}$ (SMA) – Differential reference (un-jittered) outputs, channel 3

Jit CH4B, $\overline{\text{CH4B}}$ (SMA) – Differential jittered outputs, channel 4

Ref CH3B, $\overline{\text{CH3B}}$ (SMA) – Differential reference (un-jittered) outputs, channel 3

Trig-O (SMA) – Programmable sub-rate trigger output (clk/[8,9,10,...,510,511])

Ext-Jitter (SMA) – External jitter modulation input port (DC to 100 MHz)

(GPIB) – GPIB connector, conforms to IEEE 488.1 mechanical specification

(unmarked circular 5-pin DIN) – DIN-connector for N4963A power supply

3.2.2 Label

SN (white area) – N4963A serial number

3.2.3 Controls

GPIB (switch panel) – N4963A GPIB address (down is '0', up is '1', LSB is on the left)
(Default GPIB address as shipped from the factory is 16)

Power (switch) – N4963A is powered on when switch is togged up towards 'Power' label

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4 System Details and Performance Specifications

Specifications describe the instrument's warranted performance. Non-warranted values are stated as typical. All specifications are valid in a range from 10C to 40C ambient temperature after a 30 minute warm-up phase.

The clock output channels are grouped in differential pairs. When a single port of a differential pair is used in a single-ended method of measurement, the complementary port must be terminated with a 50Ω-terminated connector.

4.1 General

Table 2. General and mechanical parameters of N4963A

Operating Temperature	+10°C to +55°C
Storage Temperature	-40°C to +70°C
Power Requirements	45W External AC Adaptor (included) • 85-265 VAC, 47-63 Hz
Physical Dimensions	Width: 254mm, Height: 63.5 mm, Depth: 254 mm
Weight	7.5lbs
EMC	Complies with European EMC Directive 2004/108/EC • IEC/EN 61326-1 • CISPR Pub 11 Group 1, class A • AS/NZS CISPR 11 • ICES/NMB-001 This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.

4.2 Safety and Regulatory

WARNING **Do not remove instrument covers. There are no user serviceable parts within. Operation of the instrument in a manner not specified by Keysight Technologies may result in personal injury or loss of life.**

WARNING **To prevent electrical shock, disconnect instrument from mains before cleaning. Use a dry cloth or one slightly dampened with water to clean the external case parts. Do not attempt to clean internally.**

WARNING **For continued protection against fire hazard, replace fuses, and or circuit breakers only with same type and ratings. The use of other fuses, circuit breakers or materials is prohibited.**

CAUTION The Mains wiring and connectors shall be compatible with the connector used in the premise electrical system. Failure, to ensure adequate earth grounding by not using the correct components may cause product damage, and serious injury.

4.3 Internal clock

The internal clock is generated by a fractional-N phase-locked loop (PLL) locked to a user-selectable internal or external 10 MHz reference clock.

The PLL multiplies the reference clock up to the high-frequency (HF) output rate. The internal reference clock is specified in Table 3.

Table 3. Parameters for N4963A 10 MHz reference

Frequency	10 MHz
Internal Reference:	20 MHz TXCO divided to 10 MHz
Accuracy	+/- 3.0 ppm from –30 to 70C internal temperature
Aging	1.0 ppm/year at 40C internal temperature
Reference Input Sensitivity (Vpp)	500 mV min. to 5 V max.
Reference Output Amplitude (Vpp)	950 mV with Internal Reference 1 V into 50 Ω with a 4 V External Reference Input
Reference Connector	Female BNC, single-ended, AC coupled, 50 Ω impedance

The clock synthesizer 13.5 GHz operates to 13.5 GHz.

The HF clock signal is split into three paths: an un-jittered reference path, an optionally jittered path, and a trigger output. See the block diagram in Figure 2.

The un-jittered reference path is available from the front-panel CH1 differential outputs, and from the rear-panel CH3A and CH3B differential outputs. CH1 has a programmable phase skew relative to all the other channels, programmable output amplitude, and programmable DC offset. CH3A and CH3B share the same programmable output amplitude.
See Table 4.

If the synthesizer is built with jitter injection, N4963A-101, the jittered high-frequency signal will be available from the front-panel CH2 differential outputs and the rear-panel CH4A and CH4B differential outputs. CH2 has programmable output amplitude and programmable DC offset. CH4A and CH4B share the same programmable output amplitude. See Table 4.

With N4963A-101, jitter can be internally generated or supplied externally. Without N4963A-101, the un-jittered reference clock is available from CH2, CH4A, and CH4B.

Table 4. Parameters for N4963A 10 MHz reference

Frequency	500 MHz to 13.5 GHz			
Frequency resolution	Front Panel		GPIB	
	1 MHz		1 KHz	
Frequency accuracy	±20 ppm			
Phase noise (typical) Output frequency=10 GHz	-65 dBc/Hz at 100Hz offset -70 dBc/Hz at 1KHz offset -75 dBc/Hz at 10KHz offset -95 dBc/Hz at 100KHz offset			
Differential output Channel	Channel 1 (front)	Channel 2 (front)	CH3A, CH3B (rear)	CH4A, CH4B (rear)
Channel type/path	Reference	Jittered	Reference	Jittered
Amplitude (Vpp) *				
0.5 to 7.5 GHz	0.6 to 2.0	0.6 to 2.0	0.2 to 0.8	0.2 to 0.8
7.5 to 13.5 GHz	0.6 to 1.5	0.6 to 1.5	0.2 to 0.6	0.2 to 0.6
Step size (mV)	1	1	1	1
DC offset (V) **	-2 to +2	-2 to +2		
Step size (mV)	10	10		
Output coupling	DC	DC	AC	AC
Phase adjust (degrees)	0 to 360			
Connector	Female-SMA	Female-SMA	Female-SMA	Female-SMA

* Both ports of differential output terminated into passive 50 Ω loads

** Maximum DC source and sink current is 50 mA (+/- 2.5 v into 50 Ω)

The third high-speed clock is internally divided by a programmable divider and then is available from the trigger output port. The divide modulus can be selected as an integer value between 8 and 511; the output waveform duty cycle varies with divide ratio. See Table 5.

Table 5. Parameters for N4963A programmable trigger output

Trigger frequency	(Clock Frequency) / (Trigger Divider Modulus)
Divider modulus range	8 to 511
Output amplitude	900 mV pp
Connector	Female-SMA, single-ended, AC coupled, 50 Ω impedance

4.4 Jitter injection

Internal and external jitter injection capability is only available when the unit is built with N4963A-101. It may be possible to upgrade your clock synthesizer to include N4963A-101, contact http://www.keysight.com/find/assist for more information.

When manufactured with N4963A-101, the front panel CH2 and rear panel CH4A and CH4B are optionally jittered with either an internal or external jitter modulation signal. The modulation signal is frequency modulated onto the high-frequency clock.

Without N4963A-101, CH2, CH4A, and CH4B supply non-jittered reference clocks.

4.4.1 Internal Jitter

The jitter modulation signal can be generated by an internal source within the clock synthesizer. Internal low frequency jitter is generated from a lookup table in the FPGA, internal high frequency jitter is generated from a Direct Digital Synthesizer (DDS).

To use internal jitter injection, press the jitter select button and select Int Jitter. Set the modulation frequency by adjusting the JITTER FREQ menu option. Set the amount of jitter by scrolling down until the MORE menu option is selected and “J xx.xui” is shown on the display.

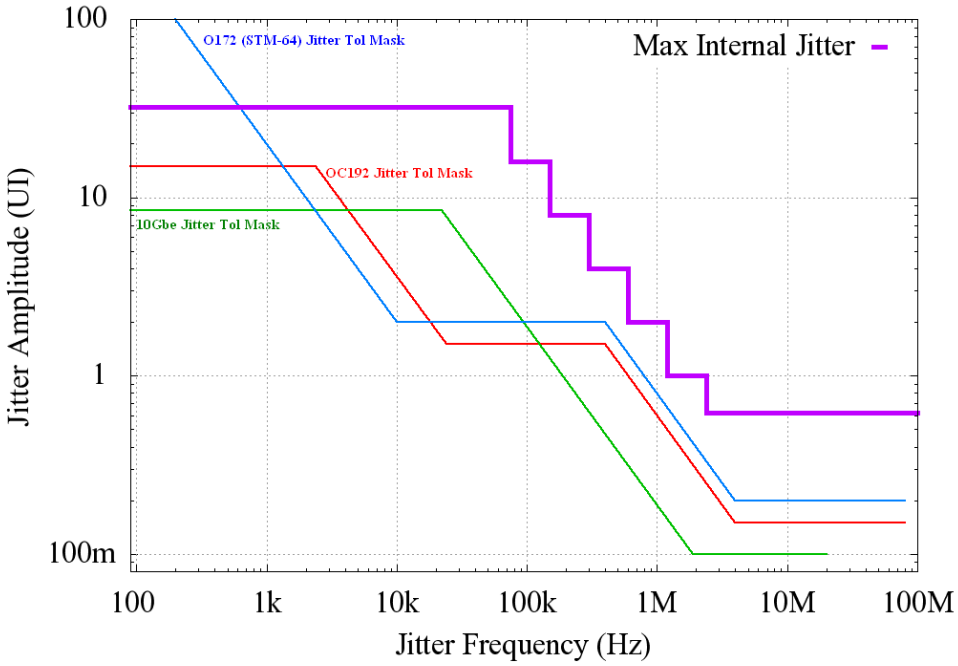

Figure 5. Maximum internal jitter generation vs. frequency

When using the internal jitter source, the method of generation is automatically selected based on the modulation frequency selected. However, different generation methods allow different amounts of jitter to be injected. Figure 5 and Table 6 indicate the maximum amount of jitter UI as a function of jitter modulation frequency.

Table 6. Parameters for N4963A internal jitter injection

Jitter frequency	1 Hz to 75 kHz	75 kHz to 2.4 MHz	2.4 MHz to 100 MHz
Maximum UI	32	16 -> 1	0.6
Jitter frequency resolution	Front Panel and GPIB		
	1 Hz in 1 Hz to 1 MHz; 1 kHz in 1 MHz to 100 MHz		
Jitter frequency accuracy	±50 ppm		
UI resolution	1 Hz to 100 MHz		
	0.01 UI		

4.4.2 External jitter

The jitter modulation signal may also be externally supplied by applying a signal to the external jitter port. Low frequency jitter signals are sampled by an ADC, and the jitter modulation signal is generated from a lookup table in the FPGA. High frequency signals are directly modulated onto the high-frequency clock.

To use external jitter injection, press the jitter select button and select Ext Jitter. Next, indicate the low or high frequency mode desired by selecting *JITTER FREQ* menu option and setting the mode. “Ext HI” will select the high-frequency mode, “Ext LO” will select the low-frequency mode. The amplitude of the external signal determines the amount of jitter injected (UI), while the frequency of the external signal determines the modulation rate.

In “Ext LO” mode, a scaling factor is used to generate high-UI jitter. The UI/volt scaling factor is available through the MORE menu option, the display will read “ExtUI=xx”. Adjust the scaling factor to generate the desired amount of UI for an input amplitude. In “Ext LO” mode, multiple UI deviation is possible by either increasing the amplitude of the applied signal or by increasing the deviation scaling factor.

The low- and high-frequency external jitter injection methods overlap, but do not count on the unit operating properly outside the specified frequency band. Also note that if the scaling factor is set higher than 1, the amount of UI injected will step when toggling between low and high frequency modes. Figure 6 and Table 7 indicate the maximum UI deviation as a function of jitter frequency.

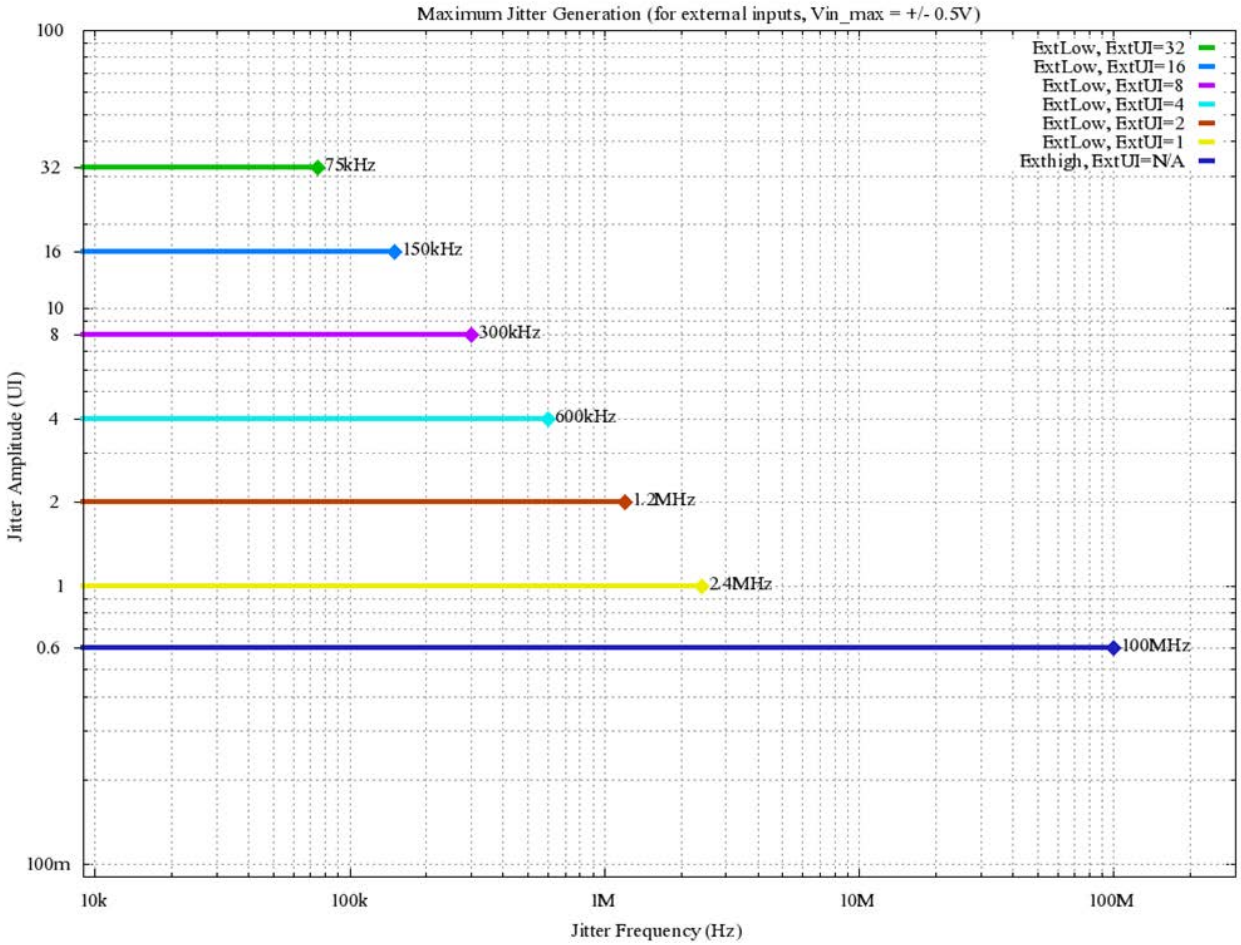

Figure 6. Maximum external jitter generation vs. frequency

Table 7. Parameters for N4963A external jitter injection

Modulation Source	External Signal Generator	
Maximum input	1 V pp	
Input	Female-SMA, Single-Ended, DC-Coupled, 50 Ω	
Deviation scaling factors	1, 2, 4, 8, 16 and 32	
	Modulation Frequency	Maximum UI
Ext. High	DC -> 100 MHz	0.6
Ext. Low; ExtUI=32	DC -> 75 kHz	32
Ext. Low; ExtUI=16	DC -> 150 kHz	16
Ext. Low; ExtUI=8	DC -> 300 kHz	8
Ext. Low; ExtUI=4	DC -> 600 kHz	4
Ext. Low; ExtUI=2	DC -> 1.2 MHz	2
Ext. Low; ExtUI=1	DC -> 2.4 MHz	1

5 Operation

The following section provides more detailed information regarding the use of the N4963A clock synthesizer 13.5 GHz. Please refer to the front and rear panel quick reference, in Section 3, for abbreviated information. The “Getting Started with the Keysight Technologies N4963A Clock Synthesizer” introduction at the front of the user guide may also prove useful.

5.1 General information

The N4963A clock synthesizer 13.5 GHz should be used in accordance with the following:

- Read and follow operating instructions; do not exceed min/max specifications.
- Use ESD protection at all times, but especially when handling RF input/outputs; ground coaxial cable conductor pins before use to remove static buildup.
- Situate the instrument away from heat sources.
- Do not block airflow to the fan; do not allow foreign material into enclosure.
- Always use provided AC adaptor. Do not power the unit with a different adaptor. Do not modify the power plug or wall outlet to remove the third (ground) pin.
- Do not drop or shake the instrument; minimize vibration; handle with care.
- There are no user-serviceable parts within. Return damaged instruments for factory-authorized repair. Refer to instrument warranty for more information.

5.1.1 Performance recommendations

Follow the following recommendations for best performance:

1. When using differential mode connection for OUT/$\overline{\text{OUT}}$,ensure the cables are phase balanced. If the electrical length of one cable is a significant fraction of a unit interval longer than the other, the quality of the differential signal will be degraded.
2. Keep cable lengths short and minimize number of cable bends.
3. When using a single port of differential output channel for single-ended measurements, the complementary port must be terminated with a 50 Ω termination.

5.1.2 Command Structure

The N4963A clock synthesizer 13.5 GHz features high-quality SMA connectors for the front and rear panel Input and Output, RF connections. Connector damage will degrade signal fidelity.

Keysight Technologies also recommends the following:

- Use a 7 to 10 in-lbs torque wrench when attaching connectors.
- Consider using connector savers to prolong performance and minimize damage.
- Differential connectors may be used single-ended if second end terminated in 50 Ω.

Inspect the connectors for the following:

- Worn or damaged threads
- Scratches to mating surface
- Burrs and loose metal particles
- Dust or foreign material in the space surrounding the center pin (type K only)
- Ensure that female contacts are straight and aligned

Clean the connectors as described in the following procedure. Cleaning connectors with alcohol shall only be done with the instruments power cord removed, and in a well-ventilated area. Allow all residual alcohol moisture to evaporate, and the fumes to dissipate prior to energizing the instrument.

1. Remove any dust or loose particles using a low-pressure air source.
2. Moisten a lint-free swab with isopropyl alcohol. Do not saturate the swab.
3. Minimize the wicking of the alcohol into the connector structure.
4. Clean the mating plane surfaces and threads.
5. Allow alcohol to evaporate, and then use a low-pressure air source to blow surfaces clean.
6. Make sure no particles or residue remains.
7. Inspect connector for damage.

5.2 Front Panel Interface

Figure 7. N4963A front panel

The N4963A front panel indicates the system configuration and can be used for local operation of the instrument. The front panel contains four groupings of buttons and lights:

1. Local status, clock output status, and 10 MHz reference path controls;
2. Jitter source control;
3. Configuration adjustment controls; and
4. Display selection controls.

The front panel also contains an eight character LED display and output unleveled LED. The front panel outputs are Channel 1, a differential reference clock output, and Channel 2, a differential jittered clock output. The front panel outputs allow for DC offsets and are therefore DC coupled.

Both outputs are available for use in single-ended or differential applications. To use the connector pairs in a single-ended configuration, terminate the unused RF connector with a 50Ω termination. For differential applications, ensure the cables used are phase balanced.

The reference output signal is described in Section 4.2 and clock jittering is described in section 4.3.

5.2.1 Display panel

Figure 8. N4963A front panel – Display panel

Table 8. N4963A front panel – Display panel

Text	Type	Description	Default
Unleveled	LED light	The unleveled indicator is lit when any of the clock outputs reach a level where they are un-calibrated.	Off
	8-digit display panel	The eight-character display shows the current configuration option selected by using the *Display->*Scroll UP and DOWN buttons. When one of the configuration *Adjust* buttons are selected, the display will show the corresponding configuration setting.	Freq (GHz)

5.2.2 Local, Clock, Reference, and Jitter Select Controls

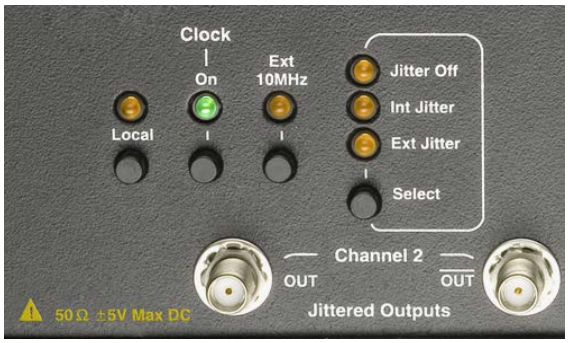

Figure 9. N4963A front panel – local, receiver, and data path controls

Table 9. N4963A front panel – local, receiver, and data path controls

Text	Type	Description	Default
Local	button & light	Light indicates local control: • ON when front-panel control is enabled; • OFF when remote GPIB interface is in use. Button switches to local control.	On
Clock -> On	button & light	Light indicates whether the output is enabled, and a signal is present at the clock outputs.	Off
Ext 10 MHz	button & light	Light indicates the synthesizer reference source: • OFF when 10 MHz source is internal • ON when 10 MHz source is external	Off

Text	Type	Description	Default
Select ->Jitter Off Int Jitter Ext Jitter	button & 3 lights	Light indicates which Jitter modulation path is selected: • Jitter Off: No jitter modulation of the jittered clock outputs (CH2, CH4A and CH4B). • Int Jitter: The jitter modulation source is from the internal generator. • Ext Jitter: The jitter modulation is from an external signal applied to the Ext Jitter connector on the back panel.	Jitter Off

5.2.3 Display selection controls

Figure 10. N4963A front panel – display selection controls

Table 10. N4963A front panel – display selection controls

Text	Type	Description	Default
Display ->Scroll	UP and DOWN buttons and 6 lights	Buttons select the measurement or configuration option to display on the display panel: • UP selects the previous display item; • DOWN selects the next display item. The selection process wraps around the display options (pressing DOWN at the last item selects the first item). The display options are: • FREQ • AMP • DC OFFSET • DELAY • JITTER FREQ • MORE (multiple options within this selection)	Freq (GHz)

5.2.4 Configuration adjustment controls

Figure 11. N4963A front panel – configuration adjustment controls

Table 11. N4963A front panel – display and configuration adjustment controls

Indicator LED	8-Digit Display	Function	Units	Default
FREQ	xxx.xxxG	Displays the clock frequency. Unit – selects the frequency band Digit – selects the digit to change Value – changes the value	G-GHz M-MHz K-KHz	005.000G
AMP	A1 x.xxx	Displays the output amplitude of the selected channel. Chan – selects channel A1, A2, A3, A4 Digit – selects the digit to change Value – changes the value	Vppk	A1 0.500
DC OFFSET	O1 x.xxx	Displays the DC offset of the selected channel. Chan – selects channel O1, O2 Digit – selects the digit to change Value – changes the value	Volts	O1 0.00
DELAY	Ph1 xxx	Displays the phase offset applied to reference clock CH1. Digit – selects the digit to change Value – changes the value	degrees	90
JITTER FREQ	xxx.xxxM	Displays the internally generated modulation frequency when *Int Jitter*	M-MHz K-KHz	000.100M

Indicator LED	8-Digit Display	Function	Units	Default
		is on. Unit – selects the frequency band Digit – selects the digit to change Value – changes the value		
	Ext (LO/HI)	Indicates the low- or high-frequency mode when using an external modulation signal with *Ext Jitter* on. Value – toggles between Low and High		Ext LO
MORE	J xx.x ui	Displays the amount of UI injected when using internally-generated jitter. Value – changes the value	UI	J 00.1 ui
MORE	ExtUI=xx	Displays the scaling factor for the externally applied jitter signal when in low-frequency mode. Value – changes the value	UI/Volt	ExtUI=16
MORE	PRE=xxx	Displays the programmable divider rate for the trigger output. Value – changes the value		PRE=008
MORE	TC1C1-A	Entry into the “About this” TC1C1A menu. Value – scrolls through information		
MORE	SN #xxxx	Unit Serial Number		
MORE	Rev xxxx	Firmware revision number		

5.3 Rear Panel Interface

Figure 12. N4963A rear panel

The N4963A rear panel features connectors for four differential clock output channels, CH3A, CH3B, CH4A and CH4B. Also included are the trigger output (Trig O), the external jitter modulation input (Ext Jitter), and an input and output for the 10MHz reference clock. The rear panel also includes a 5-bit GPIB address switch, GPIB connector, power switch, power supply din connector, and a built-in cooling fan. See Figure 2 for a system block diagram.

The two differential reference (un-jittered) outputs CH3A and CH3B (both SMA) are labeled Ref. The two differential jittered outputs CH4A and CH4B (both SMA) are labeled Jit. If the synthesizer was built without N4963A-101, the panel marking will be unchanged, and the differential outputs will generate reference clocks.

Output amplitude of CH3 (CH3A and CH3B) and CH4 (CH4A and CH4B) are adjustable. The outputs are AC coupled and no DC offset is available from the rear panel outputs.

The programmable divide-by-8 to 511 sub-rate output is available from the trigger output connector Trig O (SMA), a 50 Ω, AC coupled output.

The external jitter input connector Ext Jitter (SMA) is a 50 Ω input and is DC connected. If the synthesizer was built with N4963A-101, an external signal can be applied and is frequency modulated onto the clock.

BNC connectors are supplied for the 10MHz clock reference input and output. The

input is labeled 10 MHz IN, the output is labeled 10 MHz OUT; both are AC coupled with 50 Ω impedance.

The GPIB connector and 5-bit address switch is accessible from the rear panel. All GPIB devices on the same GPIB bus must have different addresses to function together. GPIB devices are programmed by referencing the address of the device, as well as the bus type. This is detailed in Section 6.

5.4 Power-On State

The power-on state of the N4963A is set after turning the rear power switch on. The unit comes on in local mode, and is controlled by the front panel. The internal TXCO is active after turn-on and generates a 10.0 MHz reference signal for the low frequency PLL. The power-defaults for the synthesizer are shown in Table 11. The user may now use the front panel controls to change the status of the unit or issue it commands through the GPIB port. Although the synthesizer is on, no clock signal is available from the output ports and the clock on LED is off. The clock output only becomes available when the Clock On button is pressed, at which time the clock on LED is lit.

Table 12. N4963A power-on state

Setting	Power on Value	Display	Discription
Local	On	Light	Local push-button control (GPIB interface when light off)
Clock -> On	Off	Light	Clock output indicator
Ext 10MHz	Off	Light	Reference path indicator
Jitter Select	Jitter Off	3 lights	Selects jitter input source
Unleveled	Off	Light	Indicates output is un-calibrated
FREQ	5.000 GHz	Displayed	Synthesizer clock rate
AMP	0.500 V	Not Displayed	Channel output amplitudes: A1 – A4
DC OFFSET	0.000 V	Not Displayed	Front panel DC offsets: O1 and O2
DELAY	90 Degrees	Not Displayed	Channel 1 phase offset
JITTER FREQ	100 kHz	Not Displayed	Jitter modulation frequency
J 00.1ui	0.1 UI	Not Displayed	Amount of internal injected jitter
Ext UI=16	16	Not Displayed	External jitter scaling factor
PRE=008	8	Not Displayed	Trigger output divider modulus
N4963A		Not Displayed	Unit model number

Setting	Power on Value	Display	Discription
SN #xxxx		Not Displayed	Unit serial number
Rev xxxx		Not Displayed	Firmware revision number

5.5 System verification

When first using the N4963A, and before using the unit to test an external DUT, the user should first confirm that the synthesizer is generating a clock signal of the proper frequency and amplitude. The user should also check that the unit is responding properly to the front panel and GPIB commands. The following sections give examples of how the user may verify operation of the various functions using the front panel controls. This is also a good method for the new user to get familiar with the operation of the N4963A. While performing these experiments the user should refer back to section 5.2.4, Configuration Adjustment Controls; and refer back to sections 3.1 and 3.2, the front and rear panel quick reference guides. After getting familiar with the front panel controls, the user might wish to perform similar experiments using the Lab View Driver. This will assure that the box is communicating properly over GPIB..

5.5.1 Frequency and Output Amplitude

The easiest test to start with is to verify that the N4963A is generating the proper frequency and that the rear panel outputs have amplitude control. A simple experimental setup to test these functions is shown in Figure 13.

Here the rear panel outputs, CH3B and CH4B, are connected to the inputs of a sampling scope. The synthesizer trigger output is connected to the low frequency trigger input on the scope (max trigger rate is Clock frequency by 8). The complementary CH3B output is connected to the spectrum analyzer input. As we are not terminating the complementary output of CH4B it is very important to terminate this output with a 50 Ω load.

The N4963A may now be turned on. The unit will come up in local mode utilizing the internal 10 MHz reference. The display indicator is by default showing frequency and the default frequency is 5 GHz. No output is available at any of the output ports or the trigger port until the clock is turned on. Pressing the front panel Clock-On button will allow the outputs to start transmitting. The sampling scope should now be capable of triggering on the signals emanating from CH3B and CH4B ports. Further, the clock spectrum should now be visible on the spectrum analyzer.

The first test is to verify lock. The easiest way to do this is to span in on the signal peak on the spectrum analyzer. Span in until the sweep is about 100 kHz around the signal peak. The peak should remain stable at (within the ppm accuracy of the reference) and should not be wandering about the frequency indicated on the front panel display.

The may user wish to check and use his external 10 MHz Reference. This is accomplished by connecting the external reference source output to the 10 MHz In BNC on the rear panel. The external reference is activated by pressing the Ext 10 MHz button on the front panel. Using the above procedure the user should verify that the synthesizer output is now locked to the external reference. Again, the peak should remain stable at (within the ppm accuracy of the reference) and should not be wandering about the frequency indicated on the front panel display.

Readjust the spectrum analyzer start and stop frequencies to sweep from 0 Hz to 10 GHz. Using the Digit button, set the digit indicator (blinking LED) to the GHz digit. Now use the Value button to adjust the synthesizer frequency up or down in GHz increments. The user should also see the peak on the spectrum analyze move smoothly to each new programmed frequency. Further, the period of the wave form on the scope should be appropriately changing.

The next test is to check the output amplitude control. With the frequency adjusted to some desired value, scroll the display menu to the position of amplitude adjustment, AMP. Use the Chan button to select the desired channel for amplitude adjustment.

In this case select A3, for the amplitude adjustment of the signal on CH3. Use the Digit button to select the digit to increment, for this example select the 100mV position. Then use the Value button to increment or decrement the output of CH3B. The user should verify that the peak-to-peak signal amplitude on the scope is changing to each new programmed value. By changing the channel to A4, the user should similarly be able to adjust the amplitude of the signal emanating from the CH4 ports. Please note that changing the amplitude A3, changes the amplitude on all the channel 3 ports (CH3A, CH3B and their respective complements). The same is true of changing the amplitudes, A1, A2, A3 or A4, on any of the respective channels. As the user is incrementing the signal level higher, eventually the front panel Unleveled LED will light. This is an indication that the signal output is no longer calibrated to the front panel display value. The Unleveled LED will light when any of the channel outputs become un-calibrated in this manner.

In this example channels 3B and 4B were sent to the DCA, and CH3B complement as sent to the spectrum analyzer. However the experiment will work just as well with any permutation of the channels including the front panel channels.

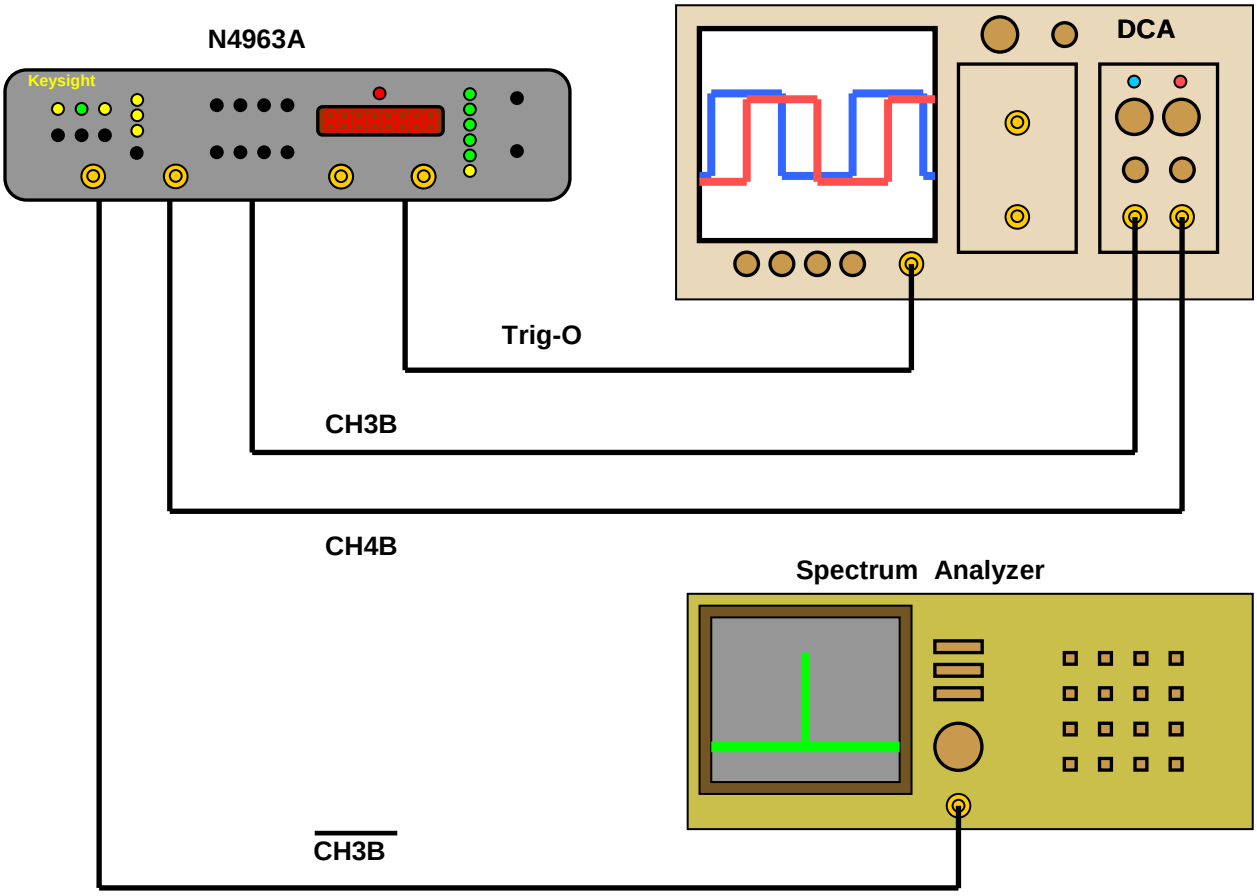

Figure 13. Frequency and output amplitude verification setup

5.5.2 DC offset and phase offset

The user should verify that the front panel amplitude adjustment control is working properly by following steps similar to those performed on the rear panel channels in the previous section. Note that the front panel output has considerably more range.

The front panel outputs have two parameter adjustments not available on the rear panel outputs. Channels 1 and 2 allow user programmable DC offset adjustments, and channel 1 has a programmable phase adjustment. The experimental set up for measuring DC offset and phase adjustment is shown in Figure 14. Here the Channel 1 and the Channel 2 complementary outputs are connected to the sampling scope. Remember to terminate, with 50 Ω terminations, the unused ports of channel 1 and 2. The trigger output is connected to the trigger input of the scope. Having verified frequency and amplitude control in the previous section, the user can set these parameters to any desired value.

The user should now scroll the display menu to the DC OFFSET position. Select channel 2, O2, for offset adjustment using the Chan button. The power-on default value is zero volts offset. Use the Digit button to select the desired digit to increment. Now use the Value button to change the offset. The channel 2 waveform on the scope should be dc level shifted with respect to the Channel 1 waveform. The measured DC offset should equal the programmed value. Try both positive and negative DC offsets. Return the Channel 2 offset to zero volts. Then use the Chan button to select channel 1, O1. Perform similar experiments adjusting the offset on channel 1 and note its DC level change with respect to the channel 2 signal on the scope. Return the channel 1 offset back to zero volts. Note that DC offset adjustment is only available for channels 1 and 2, O1 and O2 respectively.

Another experiment would be to look at only one channel. Here channel 1 and its compliment would be connected to the sampling scope. Then apply a DC offset to channel 1 and observe the effects of the offset on the Channel 1 output signal relative to its complement signal. Be sure to reconnect the system as shown in Figure 14 before performing the following delay experiment.

Now delaying the channel 1 signal relative to the other channels will be demonstrated. Scroll the display menu to the DELAY position. The delay is displayed in degrees of delay and only adjusts the delay of channel 1 with respect to the other channels. Using the Value button change the delay. As the delay is changed, the relative position of the Channel 1 signal on the scope will change with respect to the channel 2 signal. The Channel 2 signal will remain fixed. This same phase delay experiment may be repeated using a CH3 or a CH4 output in place of Channel 2. The maximum amount of phase adjustment is 358 degrees in 2 degree increments. The user may scroll through from 358 to 0 degrees or back and both the delay and display will roll over properly.

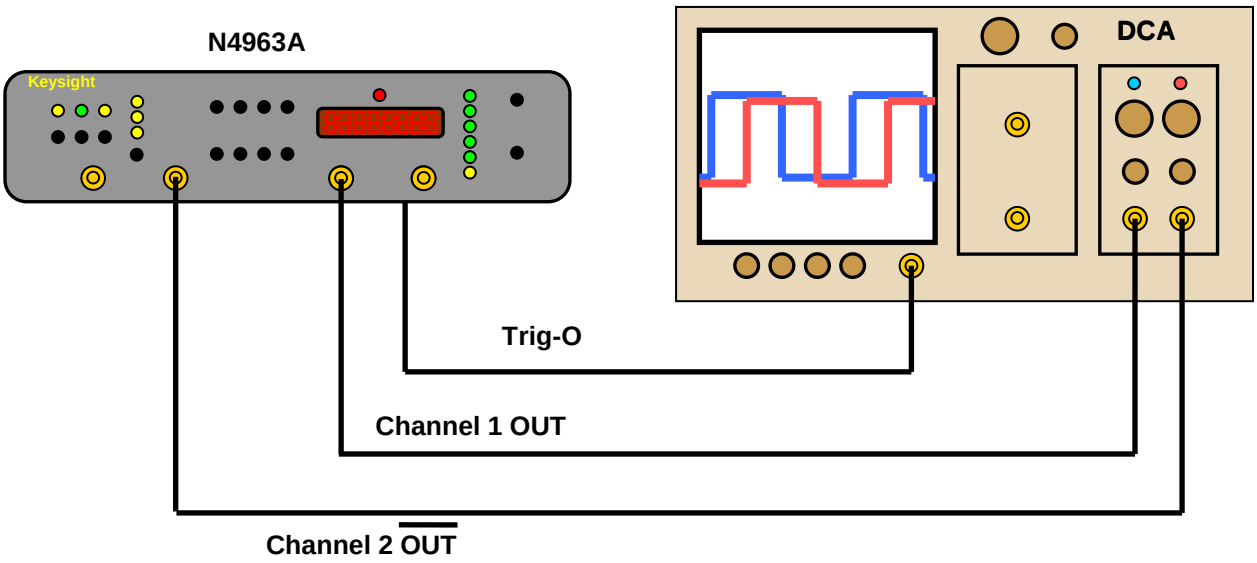

Figure 14. DC offset and phase offset verification setup

5.5.3 Internal jitter injection

The clock jitter modulation is available with N4963A-101. This option allows the user to dither the phase of the clock frequency by a user programmable amount of UI. The deviation rate is also programmable. Channels 2 and 4 (A and B) receive the jitter modulation. Channels 1 and 3 (A and 3) remain an un-jittered reference. The user can select the source of modulation to be either internal or external. This section will describe generating and measuring a jittered clock using the internal modulation source. The concepts will be similar for the external modulation. It may be useful to refer to section 4.3 describing jitter modulation.

The internal modulation source operates to two bands or modes. The low frequency mode is from 1 Hz to 1 MHz. The high frequency mode is from 1 MHz to 100 MHz. The source of the modulating signal in the low frequency mode is from an FPGA LUT. The source for the high frequency mode is a DDS. In the low frequency mode multiple UI deviation is possible. In the high frequency mode the maximum deviation is 0.6 UI. For internal jitter the N4963A switches modes automatically depending on the user programmed jitter modulation frequency.

The experimental setup is shown in Figure 15. Here the N4963A trigger output is connected to the scope trigger input. The channel 1 output is connected to the scope input and is used as a comparison reference. The jittered, complementary, Channel 2 output is connected to an external, programmable divider. The output of the divider is then connected to the sampling scope. Note, the divider must be capable of dividing at the highest clock rate (See the Keysight Technologies web page for compatible high frequency dividers). The jittered channel 2 output is connected to a spectrum analyzer.

The added divider allows the measurement of phase deviation in excess of one half UI. As the clock signal is phase modulated, its transition-edges dither back and forth about some equilibrium position. On a sampling scope these dithering transition-edges appear fuzzy or noisy. The ratio of, the time width of this edge noise to the clock period, is a measure of the phase deviation in UI. As there are 2 transition-edges per clock period it becomes impossible to measure a phase deviation of greater than half of a UI on an undivided clock signal. For deviations greater than half of a UI the signal looks completely noisy on a scope. Passing the signal through a divider does not change the time deviation of the divided clock edges, but it does extend the period of the divided signal. By increasing the divide modulus one can measure increasing numbers of UI. The maximum number of measurable UI is half the divide modulus (e.g. If the divide modulus is 4, a maximum of 2 UI can be measured on the scope). To properly see the signal on the scope, it is important that the N4963A programmable trigger divide modulus is greater than the modulus of the external divider.

After setting up the experimental configuration of Figure 15, power-on the N4963A and press the Clock-On button. Use the Select button to select internal jitter, Int Jitter. Either bypass or set the divide modulus to 1 on the external divider. This allows direct measurement of the clock jitter and period. Scroll the display menu down to JITTER FREQ, the default power-on modulating frequency is 100 kHz. This is less than 1 MHz, therefore the unit is in the low frequency mode, and programming multiple UI deviation is possible. Scroll the display down till it displays "J 00.1ui". This indicates that the power-on phase deviation is 0.1 UI. If the user compares the clock output Channel 2, transition-edge noise with that of channel 1, this added 0.1 UI of deviation will make the jitter on channel 2 greater (the transition-edges appear thicker or noisier). Use the Value button to increase the UI deviation. As the UI is increased the jitter on the transition-edges will increase. Eventually the edge jitter width is great enough that the whole signal appears blurred. At this point the external divider modulus needs to be increased (and possibly the trigger divide modulus). The amount of phase deviation is calculated by measuring the time width of the jitter and dividing by the period of the undivided clock signal. Use the value button to increment the deviation and verify that the deviation measured on the scope is consistent with the displayed value (adjust the external and trigger divide modulus as necessary). The maximum UI deviation that the N4963A is capable of producing is a function of the modulating frequency, see Figure 5.

It is not easy to measure the phase deviation or dithering rate in the time domain. However, it is much easier in the frequency domain. The deviation rate appears as side bands to the clock signal on the spectrum analyzer. Increase the deviation to several UI. Note the change in the sideband amplitudes on the spectrum analyzer. Scroll the display back to the JITTER FREQ. Now note that the sidebands are separated by the jitter frequency (100 kHz if the power-on default value is set). Increase and decrease the jitter frequency. The measured sideband separation should follow.

The user may increase the jitter frequency.First it will be noted that the maximum deviation that the N4963A can produce will decrease with increasing jitter frequency. When the programmed rate exceeds 2.4 MHz, the unit automatically switches to the high frequency mode of operation where the maximum deviation is limited to 0.6 UI. In the high frequency mode the user may measure both the Phase deviation and the deviation rate in the same manner as described above. Here the external divider modulus will never need be greater than 2, and the default trigger divide modulus of 8 will be fine.

Other techniques for making these measurements are possible. For example, complete jitter performance, both phase deviation and deviation rate, may be measured using a spectrum analyzer alone. This technique involves looking at both the relative amplitudes and the nulls of the Bessel functions determining the jitter modulation sidebands. An excellent discussion of this technique can be found in a Keysight application note called:

- Understanding Jitter and Wander Measurements and Standards 2nd Ed.

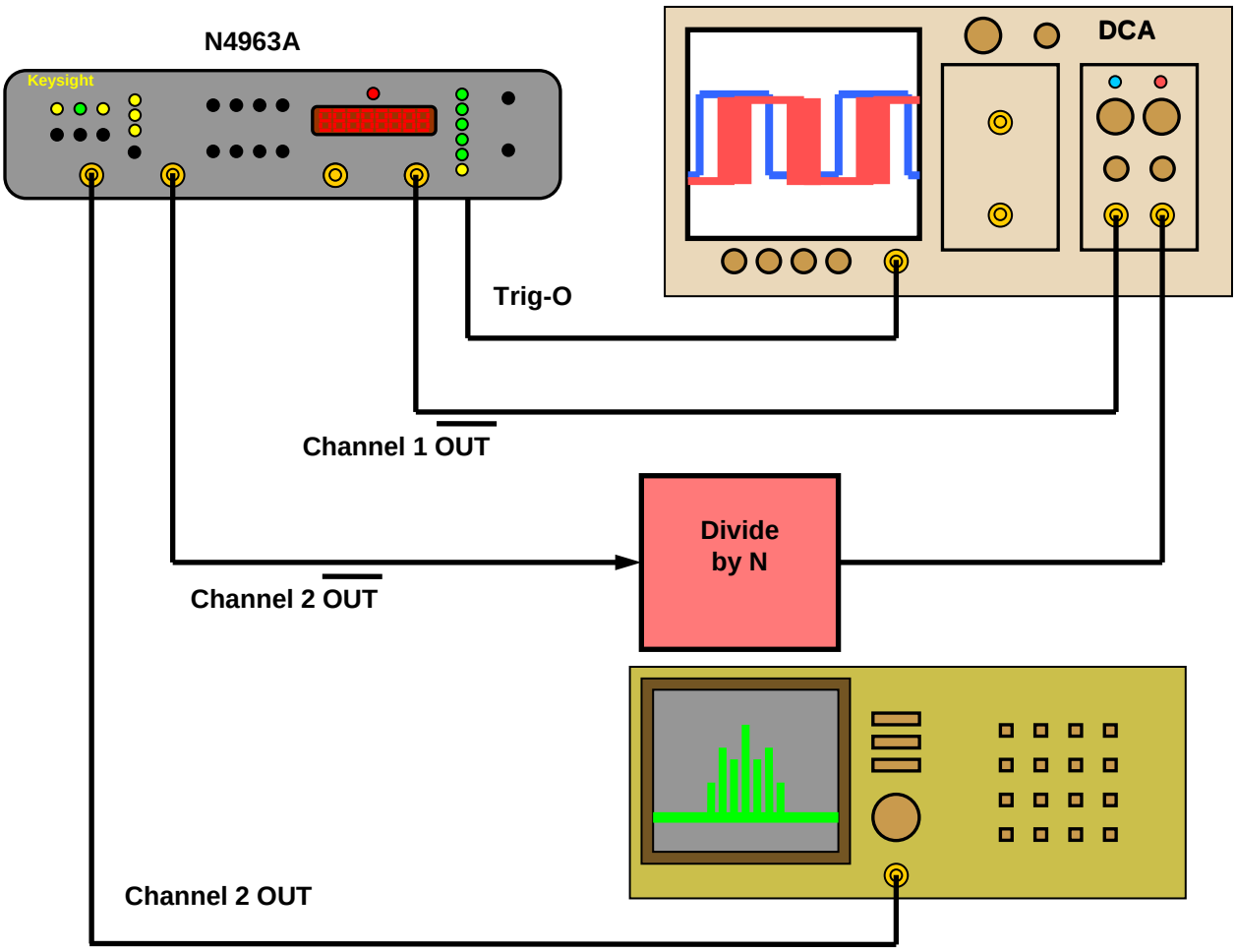

Figure 15. Internal jitter injection verification setup

5.5.4 External jitter injection

The N4963A external jitter modulation mode acts in a manner somewhat similar to the internal modulation mode. In fact the signal integrity measurement techniques are essentially the same. Therefore, it is best if the user reviews the information in the previous section, about internal modulation, and refers back to section 4.3 describing jitter modulation, before performing the experiments in this section.

The experimental set up shown in Figure 16 is very similar to the setup shown in Figure 15. New here, the output of an signal generator is applied to the external jitter input, Ext-Jitter. This source will be used to phase modulate the clock. The spectrum analyzer has been removed from the figure. However, all the comments made in the previous section about measuring phase deviation and deviation rate using the spectrum analyzer hold for this section as well.

The N4963A has two modes of operation when the jitter source is external. Like the case for internal modulation, there are low and high frequency modes. However, in this case the synthesizer does not know the frequency of the externally applied signal. It is up to the instrument operator to tell the unit in which mode to operate.

After setting up the experimental structure shown in Figure 16, power-on the N4963A and press the Clock-On button. Use the Select button to select external jitter, Ext Jitter. Before turning the external source on make sure that its amplitude level is set at its minimum. The maximum allowable signal level on the external jitter input to the N4963A is 1 V pp. Set the source frequency to some desired jitter frequency. Start with 100 kHz to make a comparison with the results from the previous section. Set “Ext LO” by scrolling the display menu down to the JITTER FREQ item. Note that the jitter frequency display indicates either “Ext LO” for low frequency mode or “Ext HI” for high frequency mode. The value button toggles the state. Make sure the unit is in low frequency mode. When using an external jitter source the amplitude of the external signal determines the phase deviation. In low frequency mode the synthesizer is capable of deviating the phase by multiple UI. The UI of phase deviation per volt of externally applied input signal is set by the external jitter scaling factor, ExtUI. Scroll the display menu down until “ExtUI=xx” is showing. Using the Value button set the parameter to 4. This tells the synthesizer that a 1 volt input should produce 4 UI of phase deviation.

Turn the external source on and adjust its output level for 1Vpp (+4 dBm) this should produce 2 UI of deviation. To measure this, set the external divide modulus to 8. This will allow the scope to display a maximum phase deviation of 4 UI. Scroll the display to the trigger pre-scalar menu item, “PRE=xxx”. Using the value button, adjust the parameter to some value greater than 8, use 16 in this case. This will allow the scope to properly trigger on the divided clock. The channel 2 waveform, on the scope, should now show a clock edge transition with 2 UI of jitter. To verify this, measure the time width of the jittered edge and divide it by the period of the undivided clock. The result should be 2. Vary the amplitude of the applied signal, the result should be a changing transition-edge jitter width. Keep in mind not to exceed the external input maximum of 1 V pp. Reduce the jitter scaling factor from 4 to 2, and the jitter width should drop in half. This is because the UI deviation per applied volt scaling factor has been reduced but not the applied signal level. As with external jitter the maximum phase deviation that the synthesizer can produce decreases with increasing frequency, see Figure 6.

With “Ext HI,” the user can always operate the external jitter injection from DC to 100MHz but the maximum deviation is only 0.6 UI.

Switching between modes “Ext LO” and “Ext HI” may produce a step discontinuity in the jitter deviation if ExtUI is not set to 01.

As in the previous section the user may verify that the jitter source frequency is indeed the phase dithering rate by using a spectrum analyzer. Measure the signal spectrum coming from any port for Channels 2 or 4. Observe the clock signal, sideband spacing is equal to the frequency of the external jitter source.

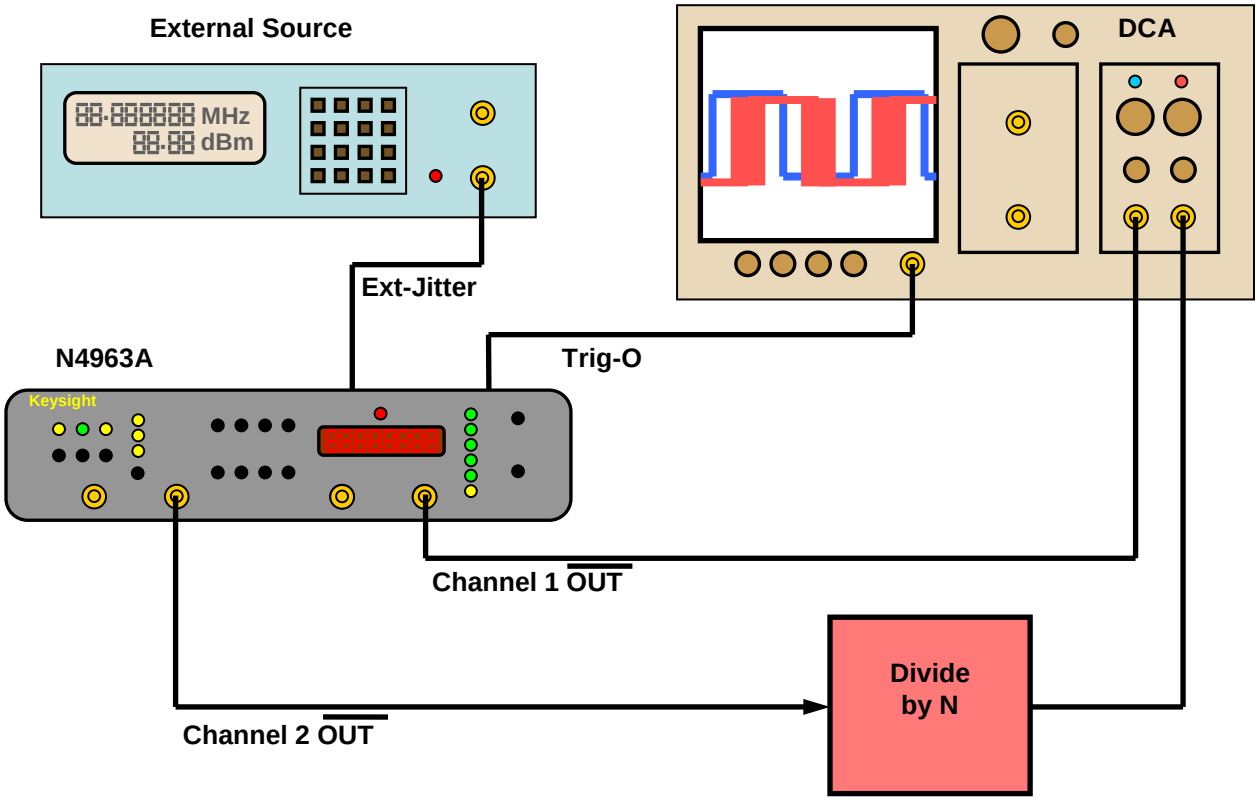

Figure 16. External jitter injection verification setup

5.6 Simple Functional Examples of N4963A use

In this section a couple of examples that utilize the N4963A as a clock source, as part of a simple measurement experiment, are given.

5.6.1 Generic test example

Generic experiment setup and description.

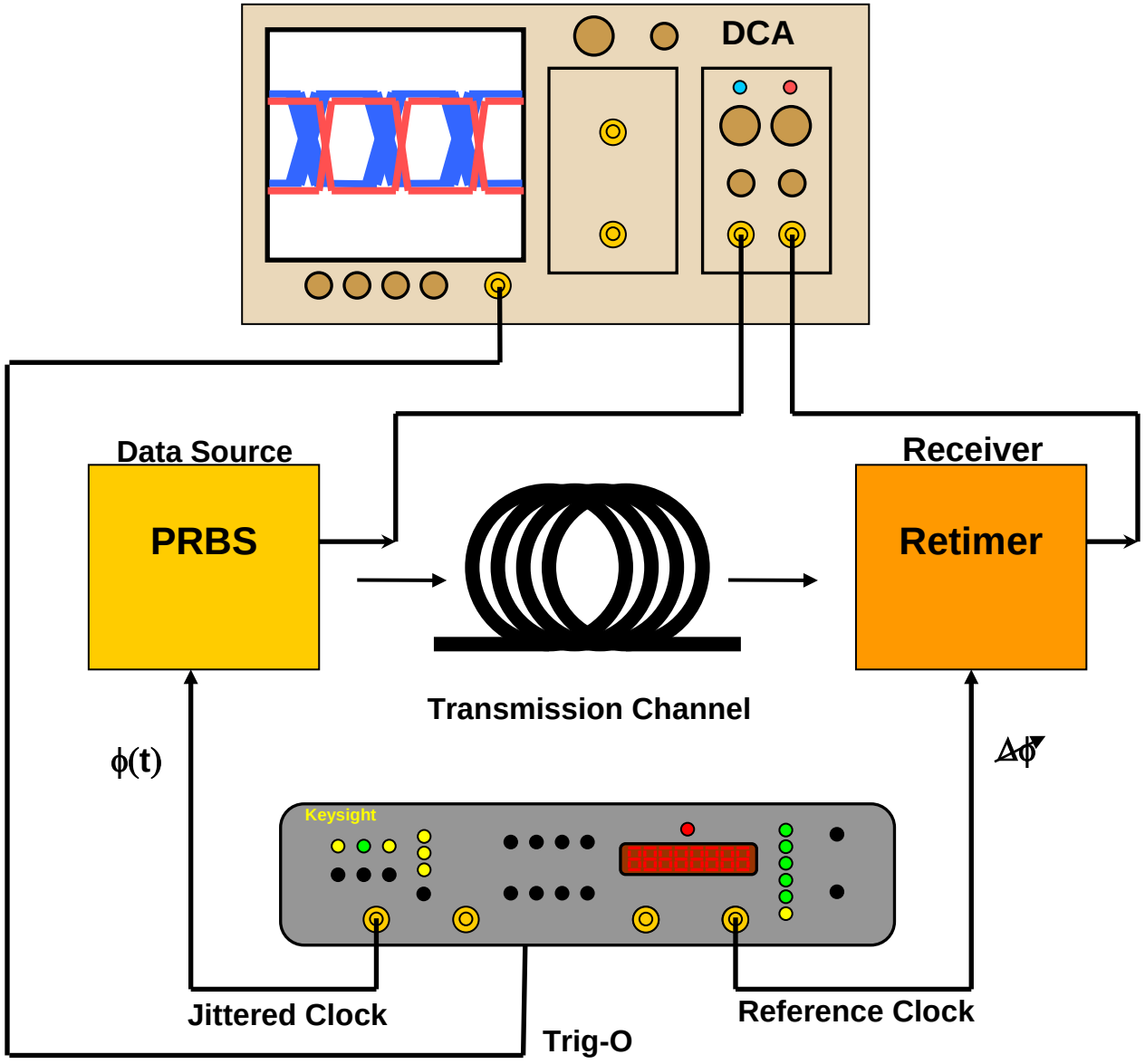

Figure 17. N4963A generic test example experimental setup

5.6.2 Example using the N4963A to Control the N4962A

Experiment setup and description of N4963A controlling the BERT.

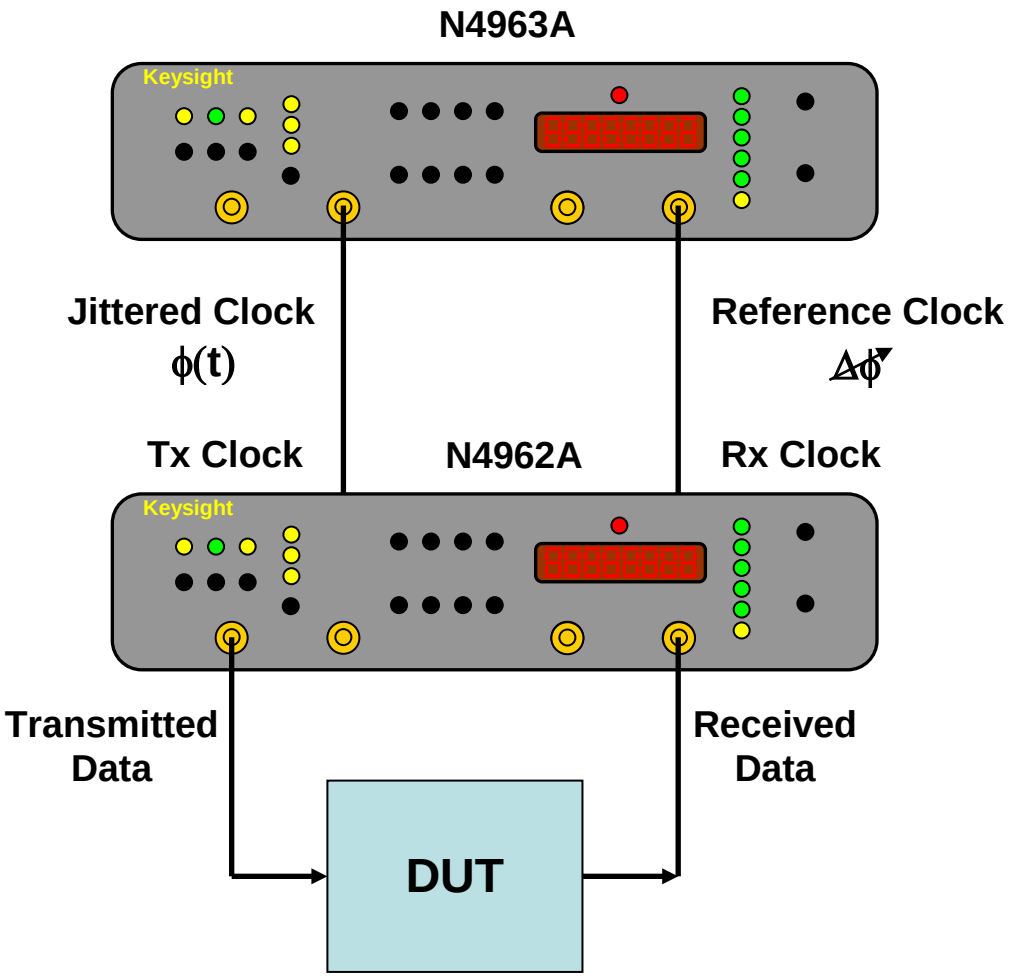

Figure 18. Experimental setup for N4962A clocked by the N4963A

6 Remote GPIB Interface

The N4963A can be controlled and queried with the rear-panel GPIB interface. The GPIB interface complies with IEEE standard 488.2-1992. To learn more about the GPIB interface, consult the following books from the IEEE:Record all symptoms.

- The International Institute of Electrical and Electronic Engineers. *IEEE Standard 488.1-1987, IEEE Standard Digital Interface for Programmable Instrumentation.* New York, NY, 1987.
- The International Institute of Electrical and Electronic Engineers. *IEEE Standard 488.2-1987, IEEE Stand Codes, Formats, Protocols and Communication Commands for Use with ANSI/IEEE Std 488.1-1987*. New York, NY, 1987.

A GPIB interface requires that all devices on a common bus have different addresses; the 5-bit address control switch is located on the back panel next to the GPIB connector, shown in Figure 12. The factory default address is 725. The address uses a three digit format. The first digit is always set to “7”, and the last two digits are programmed by the 5 bit control switch located on the back of the instrument.

6.1 GPIB Capabilities

The GPIB interface capabilities are described in Table 13.

Table 13. N4963A GPIB capabilities

Mnemonic	Function
SH1	Complete source handshake capability
AH1	Complete acceptor handshake capability
T6	Basic talker; serial poll; unaddressed to talk if addressed to listen; no talk only
L4	Basic listener; unaddressed to listen if addressed to talk; no listen only
SR1	Complete service request capability
RL2	Remote/local capability with local lockout (LLO)
PP0	No parallel port capability
DC1	Device clear capability
DT1	Device trigger capability (accepted but ignored)
C0	No controller capability
E2	Tristate outputs (except the handshake line)

6.2 GPIB Command Syntax

The N4963A can be controlled through the GPIB interface using commands and queries. The commands and queries are documented in the Backus-Naur Form notation, detailed in Table 14.

Table 14. N4963A GPIB command and query syntax

Symbol	Meaning
<>	Defined element (eg: <arg>)
::=	Is defined as (eg: <arg> ::= argument)
|	Exclusive OR
{ }	One of this group is required
[ ]	Optional item
...	Previous elements may be repeated

6.2.1 GPIB Command Syntax

The GPIB interface allows commands, which tell the instrument to take a specific action, and queries, which ask the instrument to return information.

Commands are composed of syntactic elements:

- Header – the command name; if it ends with a question mark, it is a query.
- Delimiter – a space, colon (:), comma (,), or semi-colon (;).
- Link – a command sub-function. Not all commands have links.
- Argument – a quantity, quality, or limit associated with the header or link.

Commands are case insensitive, although they are documented in an uppercase and lowercase manner that indicates which minimum characters are required to make the command. The commands can be shortened to the minimum length illustrated by the uppercase letters in the documentation.

- The command
  - **:JITTer:FREQuency?**
- Can be written in lowercase
  - **:jitter:frequency?**
- And it can be shortened
  - **:jitt:freq?**

6.3 IEEE Common Commands

The IEEE 488.2 standard has a list of reserved commands that must be implemented by all instruments using the standard. The N4963A implements all of the required commands, listed in Table 15.

Table 15. N4963A IEEE common commands

Command	Function
*CLS	Clear status command
*RST	Reset command
*WAI	Wait to continue **
*TRG?	Trigger **
*IDN?	Identification Query
*STB?	Status Byte Query
*TST?	Self Test Query **
*ESR?	Event Status Register Query
*ESE	Event Status Enable Register Set **
*ESE?	Event Status Enable Register Query **
*OPC	Operation Complete clear flag
*OPC?	Operation Complete Query
*OPT?	Option Identification Query
*SRE	Service Request Enable Set
*SRE?	Service Request Enable Query
*PSC	Power On Status Clear Flag Set **
*PSC?	Power On Status Clear Flag Set Query **
*STB?	Status Byte Query
IEEE optional commands	
*SAV	Save **
*RCL	Recall **

** Not implemented

6.4 SCPI Mandated Commands

The N4963A also conforms to the Standard Commands for Programmable Instrumentation (SCPI 1999.0) command set. Two SCPI mandated commands are implemented, listed in Table 16.

Table 16. N4963A SCPI mandated commands

Command	Function
:SYSTEM:ERROR?	Returns event/error number and message from error queue
:SYSTEM:VERSION?	Returns SCPI protocol version number ("1999.0")

6.5 N4963A Device Commands

The N4963A device commands are summarized in Table 17. The following descriptions and examples assume the user is programming with Keysight BASIC, a simple interpretative language that is convenient for instrument programming. For the examples below, the device being programmed is located at GPIB device address 725. The actual address varies according to how you have configured the GPIB bus for your own application. For information to change the bus address see Section 5.3.

Table 17. N4963A device commands

Command	Parameters/Results
:OUTPut	*{ON | OFF}*
:OUTPut?	
:FREQuency	*value <unit>*
:FREQuency?	
:SYSTem:ERRor?	
:SYSTem:VERSion?	
:AMPLitude	*Channel value <unit>*
:AMPLitude?	*Channel*
:OFFSet	*Channel value <unit>*
:OFFSet?	*Channel*
:ROSCillator	{INT | EXT}
:ROSCillator?	
:PHASe	*value*
:PHASe?	
:PREScaler	*value*
:PREScaler?	
:SOURce subsystem	
:JITTer subsystem	
:JITTer:SOURce	{ OFF | INTernal | EXTernal}

Command	Parameters/Results
:JITTer:SOURce?	
:JITTer:BAND	{ LOw | HIgh }
:JITTer:BAND?	
:JITTer:FREQuency	*value <unit>*
:JITTer:FREQuency?	
:JITTer:AMPLitude	*value*
:JITTer:AMPLitude?	
Internal Utilities	
:DACSet	*address value*
:DACSet?	
*FWREV?	

6.6 SCPI Protocol Description

The N4963A supports a simple SCPI syntax. The SCPI commands are meant to be compatible with the Keysight ESG when possible. SCPI has an associated hierarchy with it. The top level is referred as the Root mode. SCPI remembers the current hierarchy so you don't need to repeat it for subsequent commands.

6.6.1 SCPI Example

:SYSTem:REMote

:SYSTem is the root level

:REMote is the second level

The command :SYSTem would set the new default level to be the system commands.Now if the user issued a command :REMote, it would put the system into remote mode. The capital letter in :SYSTem denote the required subset of pneumonic for correct state control. The lower case letters are optional but if they are used they must be spelled correctly.

The following conventions are used in the following summary:

SYSTem - indicates that the SYST characters are required and that the keyword may optionally appear as SYSTEM instead. No other spellings are valid.

< unit> - ndicates that the unit placeholder is optional; it may or may not appear in the command.

ON | OFF - indicates a choice may be made between ON or OFF.

{ ON | OFF } - indicates that a choice must be made between ON or OFF; one or the other must appear in the command.

Numeric - the use of italics indicates that the term numeric is a placeholder in the command and is described elsewhere in the text for the command.

6.7 Command Summary

6.7.1 Root Subsystem

All of these commands can be called from the root level of the N4963A.

Command `:FREQuency numeric <unit>`

Description Set the current requested clock rate in fundamental units (Hz). Optional units include Mhz, Ghz, Hz. If no unit is specified then Hz are assumed. Exponential or floating point inputs are accepted.

Example

:FREQuency 12.5e9;	causes the clock synthesizer to generate a 12.5 GHz signal.
:FREQuency 12.5 GHz;	causes the clock synthesizer to generate a 12.5 GHz signal.
:FREQuency 12500 MHz;	causes the clock synthesizer to generate a 12.5 GHz signal.

Command `:FREQuency?`

Description Query the current clock frequency. The result is returned in Hz.

Command `:SYSTem:ERRor?`

Description Return the interrupt status or error status remotely.

Command `:SYSTEM:STATUS? CMD`

Description Where CMD is either:

"BITError" = berLed returns (1|0) if the BER led was on "NODAta" = noData returns (1|0) if there was no PRBS input "NORXclk" = ,noRxClk returns (1|0) if there was no clock on the ED "MEASdone" = Measurement Done returns (1|0) if the measurement complete "UNLOck" = sythesizer not Locked returns (1|0) internal PLL not locked "ALL"=returns integer formed with {synLock,done,noRxClk,noData, berLed}

Example :SYSTEM:STATUS? NODATA; will return a 1 if there is no input, 0 if there is valid PRBS input data

:SYSTEM:STATUS? ALL; will return an integer with {synLock, done, noRxClk,noData, berLed}

Command `*IDN?`

Description Return the model and serial numbers and the software version of the instrument as a string.

Example “KEYSIGHT TECHNOLOGIES, N4963A, SN 3001, 01.02”

Command `:AMPLitude channel value <unit>`

Description Set the specified channel amplitude to a given value. The channel output is specified as a single-ended voltage. The unit is Volts peak-to-peak. Optional <units> are V and mV.

The N4963A features four channels, 1, 2, 3, and 4. Channels 1 and 2 are the reference and jittered output channels on the front panel. Channels 3 and 4 each refer to two differential outputs on the back panel.

Command `:AMPLitude? channel`

Description Query the amplitude of the requested channel. The value is returned in Volts peak-to-peak.

Command `:OFFSet channel value <unit>`

Description Set the specified channel DC offset to the given value. The unit is DC Volts. The units which are supported are V, mV, or uV.

The reference and jittered outputs, channel 1 and channel 2, respectively, of the N4963A have DC offset control.

Example All of the following examples are valid

```
:OFFSet 1 500mV;    // set channel 1 to 0.5 V
:OFFSet 1 0.5;
:OFFSet 1 500e-3;
```

Command `:OFFSet? channel`

Description Query the DC offset of the requested channel. The value is returned in Volts.

Command `:ROSCillator { INT | EXT }`

Description Set the input used for the 10 MHz reference oscillator to internal or external mode.

Command `:ROSCillator?`

Description Query the reference oscillator for the 10MHz input. Valid response are INT, internal mode, or EXT, external mode.

Command `:PHASe value`

Description Set the phase offset of channel 1, relative to the other three channels, to a value in degrees.

Command `:PHASe?`

Description Query the phase offset of channel 1. Returns a value in degrees.

Command `:PREScaler value`

Description Set the programmable trigger prescaler to a value between 8 and 511. This sets the output rate of the trigger.
Trigger Frequency = Clock synthesizer 13.5 GHz Frequency / Prescaler value.

Command `:PREScaler?`

Description Query the value of the trigger prescaler. Returns a value between 8 and 511.

6.7.2 :SOURce Subsystem

For backward compatibility with the Keysight ESG (economy signal generator), all Keysight compatible root subsystem commands may be preceded with the SOURce subsystem.

The output on/off command is:

Command `:SOURce:OUTPut ON | OFF`

The on/off Querry :SOURce:OUTPut?

Example

:SOURce:OUTPut ON	Will turn the clock output on.
:SOURce:OUTPut?	Will find out if the output is on or off.
:SOURce:OUTPut OFF	Will turn the clock output off.
:SOURce:AMPLitude? 1	Will return the amplitude of channel 1.
:SOURCE:FREQuency?	Will return the Clock synthesizer 13.5 GHz clock rate.

6.7.3 JITTer Subsystem(N4963A 101)

The jitter subsystem requires option N4963A-101.

The jitter subsystem provides the jitter programming capabilities for the N4963A.

Command `:JITTer:SOURce { OFF | INTernal | EXTernal }`

Description Set the jitter of the N4963A. It is used to either turn the jitter off; or to set the jitter source to the internal source or to the external signal provided to the Jitter-In rear panel connector.

Command `:JITTer:SOURce?`

Description Query the jitter state of the N4963A. Returns values OFF, INT, or EXT.

Command `:JITTer:BAND { LOw | HIgh }`

Description Set the jitter path of the N4963A when using external jitter inputs. Low band signals are digitized and scaled by the ExtUI=[1|2|4|8|16|32] parameter which determines the maximum UI available with a full scale input signal. High band signals pass thru analog signal processing blocks, are limited to a reduced max UI value and do not receive any additional signal scaling.

Command `:JITTer:BAND?`

Description Query the jitter band state of the N4963A when using an external jitter input. Returns values LOW or HIGH.

Command `:JITTer:FREQuency value <unit>`

Description Set the jitter frequency of the internal periodic jitter generator to a given value. The value is in fundamental units of Hertz. An optional unit of Hz, kHz, MHz may be specified.

Example
:JITTer:FREQuency 10.3kHz;
:JITTer:FREQuency 10.3e3;

Command `:JITTer:FREQuency?`

Description Query the jitter frequency of the N4963A.

Command `:JITTer:AMPLitude value`

Description Set the jitter frequency of the internal periodic jitter generator to a given value in unit intervals UI. The minimum step for jitter UI is 0.1UI. Internally values will be rounded up to the nearest 0.1 UI. The value of the jitter is unitless and it will accept a floating point or scientific notation input.
The maximum input jitter versus jitter modulation frequency is given in Table 6

Example
:JITTer:AMPLitude 1.2
:JITTer:AMPLitude 12e-1;
:JITTer:AMPLitude 1234;
The last example would internally be rounded to 1.2 UI's of jitter.

Command `:JITTer:AMPLitude?`

Description Query the jitter amplitude of the N4963A.

6.8 IEEE Common Capabilities

This is a summary of the subset of IEEE standard GPIB commands that are implemented in the N4963A.

Command `*CLS`

Description Clear Status, clears IO stack.

Command `*ESE?`

Description Event Status Enable Query – not implemented.

Command `*IDN?`

Description Returns the manufacturers name, model number, serial number and firmware revision as a string:
"KEYSIGHT TECHNOLOGIES, N4963A, SN3001, Rev01.02"

Command `*LRN?`

Description Learn Query – not implemented.

Command `*OPC?`

Description Operation Complete will return true when a timed measurement is complete of if a command to automatically set the phase completes – not implemented.

Command `*OPT?`

Description Option Identification Query- returns the options in the instrument as a comma delimited string.

Option	Result
None	(an empty string)
13.5 GHz clock	001
Jitter Injection	002

Command `*PSC numeric`

Description Sets the value of the Power On Status Clear Flag. Controls the automatic clearing of the SRQ enable register see IEEE 488.2 Section 10.25. Not implemented.

Command `*PSC?`

Description Returns value of PSC flag. Not implemented.

Command `*RCL numeric`

Description Recall Stored Settings – not implemented.

Command `*RST`

Description Resets the instrument to power on state.

Command `*SAV numeric`

Description Save stored settings.Stores the current instrument state – not implemented.

Command `*SRE numeric`

Description Service Request Enable – Sets the status byte mask

numeric =	8	QUES Status Summary
	16	Message Available
	32	Event Status Summary
	64	Request Service
	128	OPER status summary

Command `*SRE?`

Description Service Request Enable Query.

Command `*STB?`

Description Status Byte Query – Returns the value of the status byte in numeric form.

Command `*TRG`

Description Trigger – Not implemented.

Command `*TRG?`

Description Trigger Query – not implemented.

Command `*WAI`

Description Wait to Continue – not implemented.

Command `*TST`

Description Initiate Self Test – not implemented.

Command *TST?

Description Self Test Query – not implemented.

6.9 PERL Script to exercise GPIB Commands

```
#!/usr/local/bin/perl
#
#  test all commands on N4963A
#

use RPCINST;
use strict;

my($reg)=1;
my($addr);

#create object and load with address to the unit
#add your address here

my($gpib)=RPCINST->new("192.168.100.223","hpib,16");
my($result)=$gpib->iconnect();
printf "ICONNECT result = $result \n";
my($last_string);
my($err_res);
my($exit_on_errors)=0;

sub check_errors
{
  my($res)=$gpib->iwrite(":SYSTEM:ERROR?");
  my($error)=$gpib->iread();
  if ($error =~ /No error/ ) {
    $err_res=0;
    return;
  }
  else {
    $err_res=1;
    printf("$last_string \nerror=$error\n");
    if ($exit_on_errors eq 1) { exit; }
  }
}

sub gpib_write
{
   my($string)=shift;
   $last_string=$string;
   printf("testing  $string");
   my($res)=$gpib->iwrite($string);
   #  slow writing EEPROM
   if ( ($string =~/RCL/) || ($string =~/SAV/) ) { sleep 1; }

   if ( ($string =~ /\?/) ) {
```

```
    # do nothing becuse  query
  }
  else { printf "\n";
    #  check_errors();
  }
  #  sleep 1;
  # for (my($c)=0; $c<10000; $c++) { my($wait)=1; }
  return $res;

}

sub gpib_read
{
  my($string)=shift;
  sleep 1;
  my($res)=$gpib->iread();
  printf " = $res";
  return $res;
}


$exit_on_errors=0;


my($result)=gpib_write("*IDN?");
my($idn)=gpib_read(100,200);

my($result)=gpib_write(":SSC:FREQUENCY 31KHZ");
my($result)=gpib_write(":SSC:ENABLED ON");
my($result)=gpib_write(":SSC:PERCENT 0.33 ");

while(1) {
my($result)=gpib_write(":SSC:ENABLED ON");
my($result)=gpib_write(":SSC:FREQ 31e3 ");
my($result)=gpib_write(":SSC:PERC 0.33 ");
my($result)=gpib_write(":JITTER:SOURCE OFF");
my($result)=gpib_write(":DACS 6 8");
my($result)=gpib_write(":DACS 7 8");
# my($result)=gpib_write(":OFFSET 1 0mV");
my($result)=gpib_write(":AMPL 1 50mV");
my($result)=gpib_write(":AMPL 2 50mV");
my($result)=gpib_write(":AMPL 3 50mV");
my($result)=gpib_write(":AMPL 4 50mV");
my($result)=gpib_write(":PRES 10");
my($result)=gpib_write(":OUTP ON");

my($result)=gpib_write(":FREQ 10.01  GHZ");
my($result)=gpib_write(":JITTER:AMPL  3.3 ");
my($result)=gpib_write(":JITTER:FREQUENCY 10e6 ");
my($result)=gpib_write(":ROSC EXT");
my($result)=gpib_write(":ROSC INT");
```

```
my($result)=gpib_write(":DACS 6 1000");
my($result)=gpib_write(":DACS 7 1000");
my($result)=gpib_write(":PHASE  66 ");
my($result)=gpib_write(":JITTER:SOURCE INT ");
my($result)=gpib_write(":AMPL 1 100mV");
my($result)=gpib_write(":AMPLITUDE 2 200mV;");
my($result)=gpib_write(":AMPL 3 300mV");
my($result)=gpib_write(":AMPL 4 0.40V");
# my($result)=gpib_write(":OFFSET 1 700mV");
# my($result)=gpib_write(":OFFSET 2 -200mV");
my($result)=gpib_write(":OUTP OFF");
my($result)=gpib_write(":FREQ 5 GHZ");
my($result)=gpib_write(":PHASE  22 ");
my($result)=gpib_write(":PRES 50");
my($result)=gpib_write(":JITTER:FREQUENCY 1e4 ");
my($result)=gpib_write(":JITTER:AMPL  8 ");
my($result)=gpib_write(":JITTER:SOURCE EXT");
my($result)=gpib_write(":SSC:ENABLED OFF");
my($result)=gpib_write(":SSC:FREQ 77e3 ");
my($result)=gpib_write(":SSC:PERC 0.11 ");
}
```

7 Returning the N4963A Clock Synthesizer to Keysight Technologies

If the N4963A clock Synthesizer 13.5 GHz fails system verification and you cannot correct the problem, return it to Keysight Technologies for repair following the steps shown below.

1. Record all symptoms.
2. Contact Keysight Technologies using the “Request an RMA” form at http://www.keysight.com/find/assist.
3. Use the original packing material or comparable packing material to ship the instrument to Keysight Technologies.

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