NI PXI-5422 Specifications

16-Bit 200 MS/s Arbitrary Waveform Generator

Français	Deutsch	日本語	한국어	简体中文
ni.com/manuals				

Unless otherwise noted, the following conditions were used for each specification:

- Analog filter enabled.
- Signals terminated with 50 Ω.
- Direct path set to 1 Vpk-pk, Low-Gain Amplifier path set to 2 Vpk-pk, and High-Gain Amplifier path set to 12 Vpk-pk.
- Sample rate set to 200 megasamples per second (MS/s) and the sample clock source set to Divide-by-*N*.

Typical values are representative of an average unit operating at room temperature (20 ±3 °C). Specifications are subject to change without notice. For the most recent NI 5422 specifications, visit `ni.com/manuals`.

To access all of the NI 5422 documentation, including the *NI Signal Generators Getting Started Guide*, which contains functional descriptions of the NI 5422 signals, navigate to **Start» All Programs»National Instruments»NI-FGEN»Documentation**.

Caution The protection provided by this product may be impaired if it is used in a way not specified in this document.

Hot Surface If the NI 5422 has been in use, it may exceed safe handling temperatures and cause burns. Allow the NI 5422 to cool before removing it from the chassis.

Contents

CH 0 (Channel 0 Analog Output, Front Panel Connector)

Specification	Value	Comments
Number of Channels	1	—
Connector	SMB (jack)	—
Output Voltage Characteristics		
Output Paths	1. The software-selectable Main Output path setting provides full-scale voltages from 12.00 Vpk-pk to 5.64 mVpk-pk into a 50 Ω load. NI-FGEN uses either the Low-Gain Amplifier or the High-Gain Amplifier when the Main Output path is selected, depending on the Gain attribute. 2. The software-selectable Direct path is optimized for intermediate frequency (IF) applications and provides full-scale voltages from 1.000 to 0.707 Vpk-pk.	—
DAC Resolution	16 bits	—

Specification	Value				Comments
Amplitude and Offset					
Amplitude Range	Path	Load	Amplitude (Vpk-pk) Minimum Value	Amplitude (Vpk-pk) Maximum Value	Amplitude values assume the full scale of the DAC is utilized. If an amplitude smaller than the minimum value is desired, then waveforms less than full scale of the DAC can be used. NI-FGEN compensates for user-specified resistive loads.
	Direct	50 Ω	0.707	1.00	
		1 kΩ	1.35	1.91	
		Open	1.41	2.00	
	Low-Gain Amplifier	50 Ω	0.00564	2.00	
		1 kΩ	0.0107	3.81	
		Open	0.0113	4.00	
	High-Gain Amplifier	50 Ω	0.0338	12.0	
		1 kΩ	0.0644	22.9	
		Open	0.0676	24.0	
Amplitude Resolution	<0.06% (0.004 dB) of amplitude range				
Offset Range	Span of ±50% of the amplitude range with increments <0.0028% of amplitude range				Not available on the Direct path.

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td colspan="5">Maximum Output Voltage</td></tr>
<tr><td rowspan="10">Maximum Output Voltage</td><td>Path</td><td>Load</td><td>Maximum Output Voltage (V)</td><td rowspan="10">The combination of amplitude and offset is limited by the maximum output voltage.</td></tr>
<tr><td rowspan="3">Direct</td><td>50 Ω</td><td>±0.500</td></tr>
<tr><td>1 kΩ</td><td>±0.953</td></tr>
<tr><td>Open</td><td>±1.000</td></tr>
<tr><td rowspan="3">Low-Gain Amplifier</td><td>50 Ω</td><td>±1.000</td></tr>
<tr><td>1 kΩ</td><td>±1.905</td></tr>
<tr><td>Open</td><td>±2.000</td></tr>
<tr><td rowspan="3">High-Gain Amplifier</td><td>50 Ω</td><td>±6.000</td></tr>
<tr><td>1 kΩ</td><td>±11.43</td></tr>
<tr><td>Open</td><td>±12.00</td></tr>
<tr><td colspan="5">Accuracy</td></tr>
<tr><td>DC Accuracy</td><td colspan="3">For the Low-Gain or High-Gain Amplifier path:

±0.2% of amplitude range ±0.05% of offset ±500 µV
(within ±10 °C of self-calibration temperature)

±0.4% of amplitude range ±0.05% of offset ±1 mV (0 to 55 °C)

For the Direct path:

Gain accuracy: ±0.2% amplitude range
(within ±10 °C of self-calibration temperature)
Gain accuracy: ±0.4% amplitude range
(0 to 55 °C)

DC offset error: ±30 mV (0 to 55 °C)

Note: For DC accuracy, “amplitude range” is defined as 2× the gain setting. For example, a DC signal with a gain of 8 has an amplitude range of 16 V. If this signal has an offset of 1.5, its DC accuracy is calculated by the following equation:

$\pm 0.2\% \times (16\text{ V}) \pm 0.05\% \times (1.5\text{ V}) \pm 500\ \mu\text{V} = \pm 33.25\text{ mV}$</td><td>All paths are calibrated for amplitude and gain errors. The Low-Gain and High-Gain Amplifier paths also are calibrated for offset errors. Calibrated for high-impedance load.</td></tr>
</table>

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>AC Amplitude Accuracy</td><td colspan="3">±1.0% of desired Amplitude ± 1 mV</td><td>50 kHz sine wave. Signals terminated with high impedance.</td></tr>
<tr><td colspan="5">Output Characteristics</td></tr>
<tr><td>Output Impedance</td><td colspan="3">50 Ω nominal or 75 Ω nominal, software-selectable</td><td>—</td></tr>
<tr><td>Output Coupling</td><td colspan="3">DC</td><td>—</td></tr>
<tr><td>Output Enable</td><td colspan="3">Software-selectable. When the Output Path is disabled, the CH 0 output is terminated to ground with a 1 W resistor equal to the selected output impedance.</td><td>—</td></tr>
<tr><td>Maximum Output Overload</td><td colspan="3">The CH 0 output can be connected to a 50 Ω, ±12 V (±8 V for the Direct path) source without sustaining any damage. No damage occurs if the CH 0 output is shorted to ground indefinitely.</td><td>—</td></tr>
<tr><td>Waveform Summing</td><td colspan="3">The CH 0 output supports waveform summing among similar paths—specifically, the outputs of multiple NI 5422 signal generators can be connected directly together.</td><td>—</td></tr>
<tr><td colspan="5">Frequency and Transient Response</td></tr>
<tr><td>Analog Filter</td><td colspan="3">Software-selectable 7-pole elliptical filter for image suppression</td><td>Available on Low-Gain Amplifier and High-Gain Amplifier paths.</td></tr>
<tr><td rowspan="2">Pulse Response</td><td colspan="3">Path</td><td rowspan="4">Values are typical. Analog Filter disabled. Measured with a 1 m RG-223 cable.</td></tr>
<tr><td>Direct</td><td>Low-Gain Amplifier</td><td>High-Gain Amplifier</td></tr>
<tr><td>Rise/Fall Time</td><td>1.0 ns</td><td>2.1 ns</td><td>4.8 ns</td></tr>
<tr><td>Aberration</td><td>16%</td><td>6%</td><td>8%</td></tr>
</table>

Figure 1. Normalized Passband Flatness, Direct Path

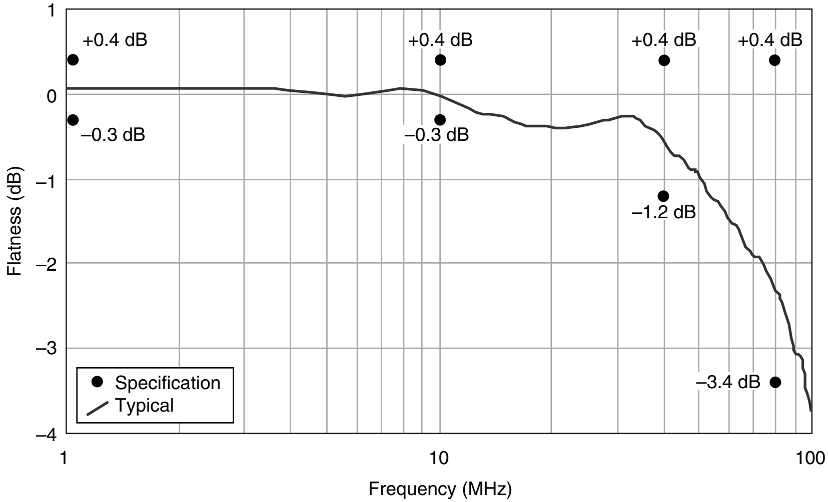


Figure 2. Normalized Passband Flatness, Low-Gain Amplifier Path

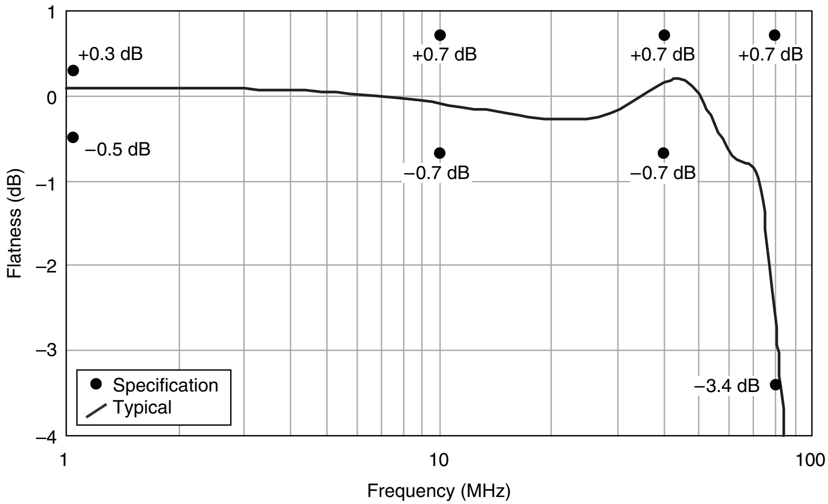


Figure 3. Normalized Passband Flatness, High-Gain Amplifier Path

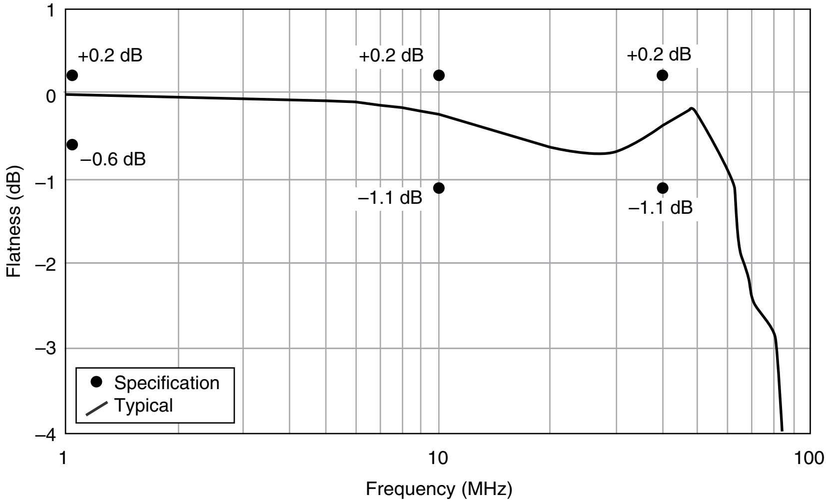
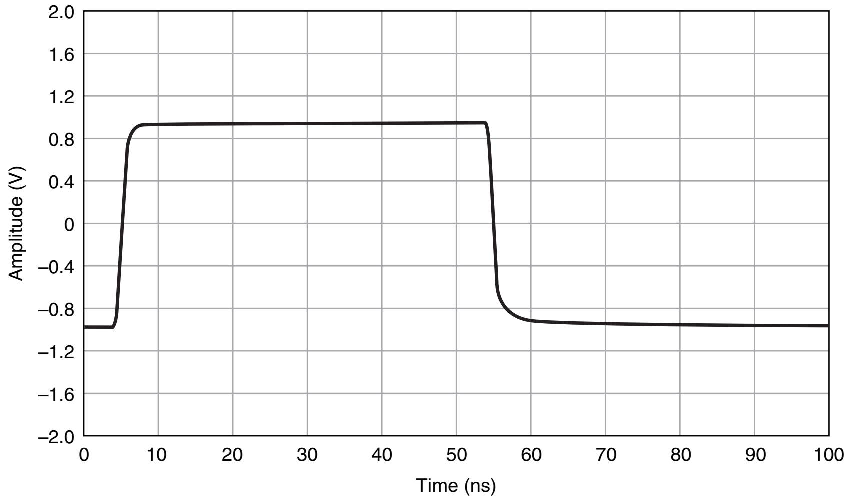
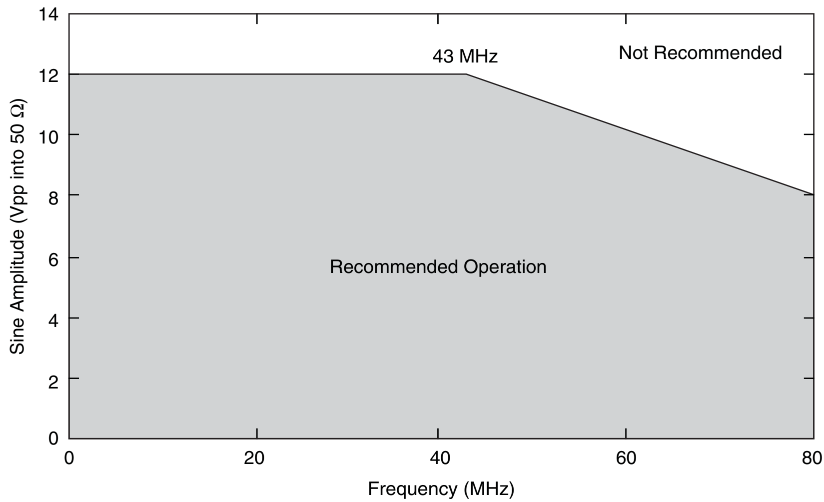


Figure 4. Pulse Response, Low-Gain Amplifier Path with a 50 Ω Load



Specification	Value			Comments
Suggested Maximum Frequencies for Common Functions				
	Path			
Function	Direct	Low-Gain Amplifier	High-Gain Amplifier	Disable the Analog Filter for square, ramp, and triangle functions. The minimum Frequency is <1 mHz. The value depends on memory size and device configuration.
Sine	80 MHz	80 MHz	43 MHz	
Square	Not Recommended	50 MHz	25 MHz	
Ramp	Not Recommended	10 MHz	10 MHz	
Triangle	Not Recommended	10 MHz	10 MHz	

Figure 5. Amplitude Versus Recommended Sine Wave Frequency

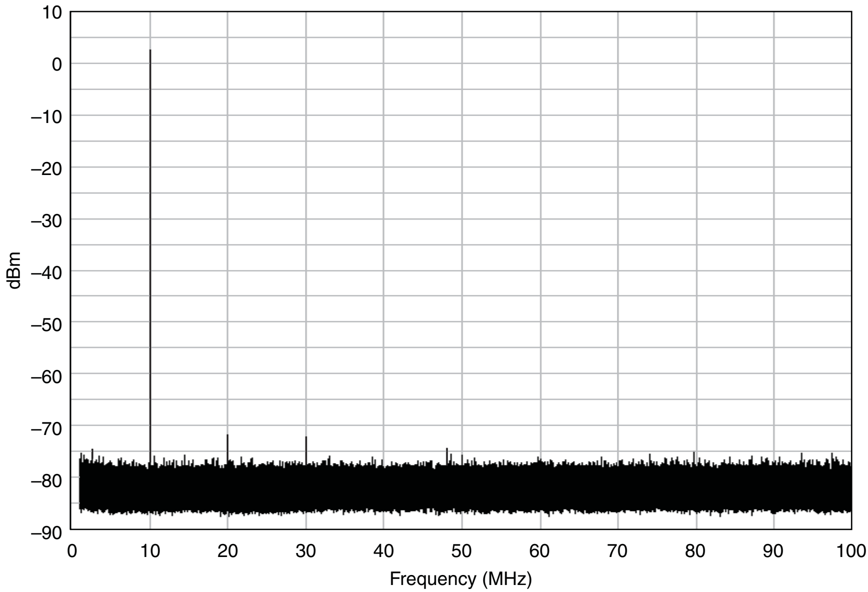


Specification	Value			Comments
Spectral Characteristics				
Spurious-Free Dynamic Range (SFDR)* with Harmonics	Path			Amplitude -1 decibel full scale (dBFS). Measured from DC to 100 MHz. All values are typical and include aliased harmonics.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	70 dB	65 dB	66 dB	
5 MHz	70 dB	65 dB	58 dB	
10 MHz	70 dB	65 dB	52 dB	
20 MHz	63 dB	64 dB	49 dB	
30 MHz	57 dB	60 dB	43 dB	
40 MHz	48 dB	53 dB	39 dB	
50 MHz	48 dB	53 dB	—	
60 MHz	47 dB	52 dB	—	
70 MHz	47 dB	52 dB	—	
80 MHz	41 dB	52 dB	—	
SFDR without Harmonics	Path			Amplitude -1 dBFS. Measured from DC to 100 MHz. All values are typical and include aliased harmonics.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	84 dB	79 dB	76 dB	
5 MHz	84 dB	79 dB	76 dB	
10 MHz	79 dB	79 dB	76 dB	
20 MHz	79 dB	79 dB	76 dB	
30 MHz	72 dB	70 dB	67 dB	
40 MHz	47 dB	57 dB	54 dB	
50 MHz	47 dB	52 dB	—	
60 MHz	46 dB	51 dB	—	
70 MHz	46 dB	51 dB	—	
80 MHz	40 dB	51 dB	—	

* Dynamic range is defined as the difference between the carrier level and the largest spur.

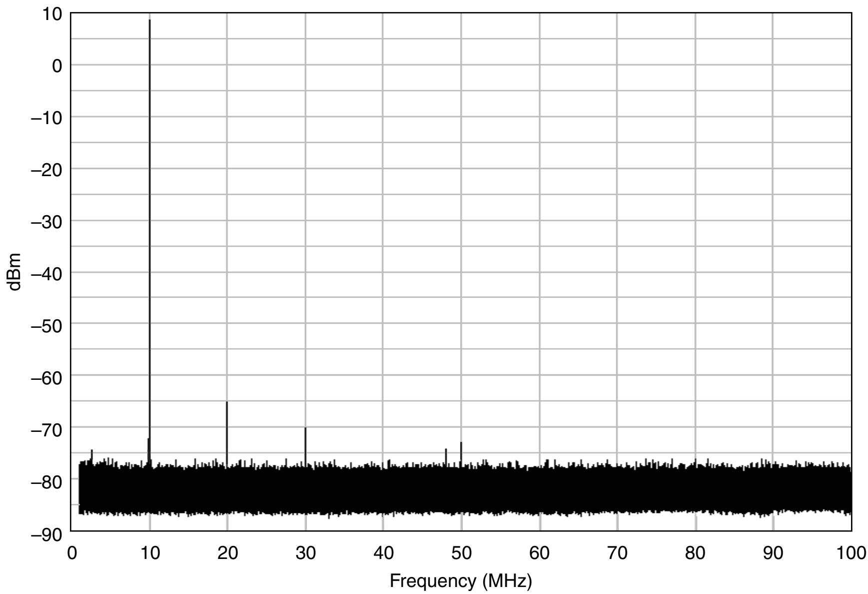
Specification	Value						Comments
		Amplitude Range		Average Noise Density			
	Path	Vpk-pk	dBm	$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz	
Average Noise Density	Direct	1.00	4.0	19.9	-141	-145	Average noise density at small amplitudes is limited by a -148 dBm/Hz noise floor. All values are typical.
	Low Gain	0.06	-20.5	1.3	-148	-144	
	Low Gain	0.10	-16.0	2.2	-148	-144	
	Low Gain	0.40	-4.0	8.9	-148	-144	
	Low Gain	1.00	4.0	22.3	-140	-144	
	Low Gain	2.00	10.0	44.6	-134	-144	
	High Gain	4.00	16.0	93.8	-128	-144	
	High Gain	12.00	25.6	281.5	-118	-144	

Figure 6. 10 MHz Single-Tone Spectrum, Direct Path, 200 MS/s (Typical)



Note The noise floor in Figure 6 is limited by the measurement device. Refer to the *Average Noise Density* specification for more information about this limit.

Figure 7. 10.00001 MHz Single-Tone Spectrum, Low-Gain Amplifier Path, 200 MS/s (Typical)



Note The noise floor in Figure 7 is limited by the measurement device. Refer to the *Average Noise Density* specification for more information about this limit.

Figure 8. Total Harmonic Distortion, Direct Path (Typical)

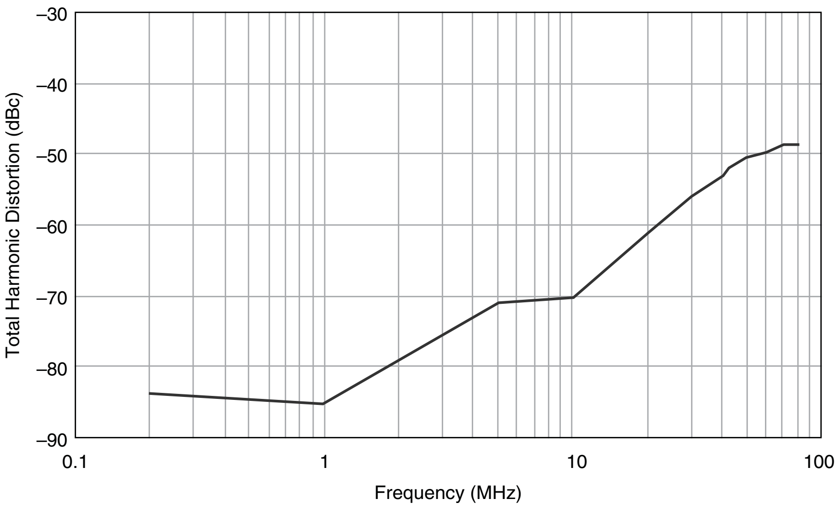


Figure 9. Total Harmonic Distortion, Low-Gain Amplifier Path (Typical)

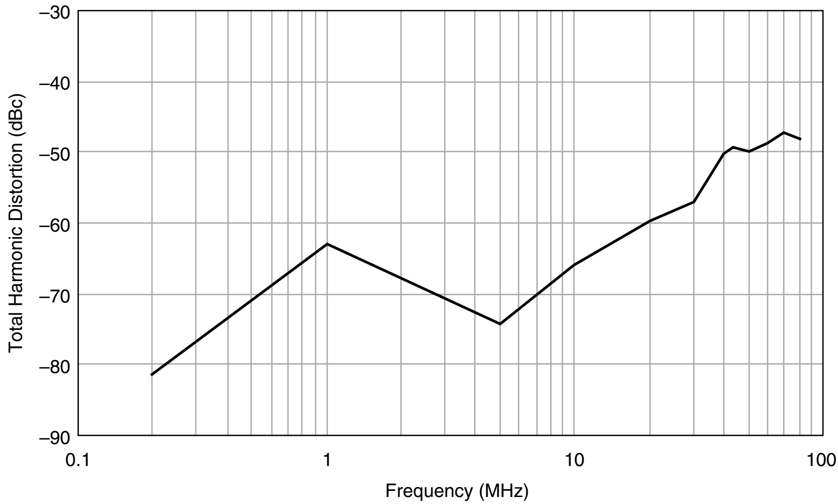


Figure 10. Total Harmonic Distortion, High-Gain Amplifier Path (Typical)

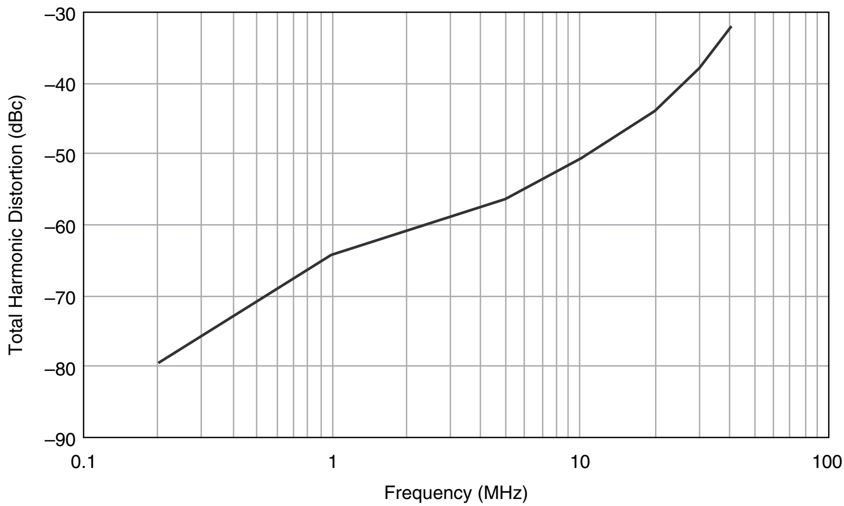


Figure 11. Intermodulation Distortion, 200 kHz Separation (Typical)

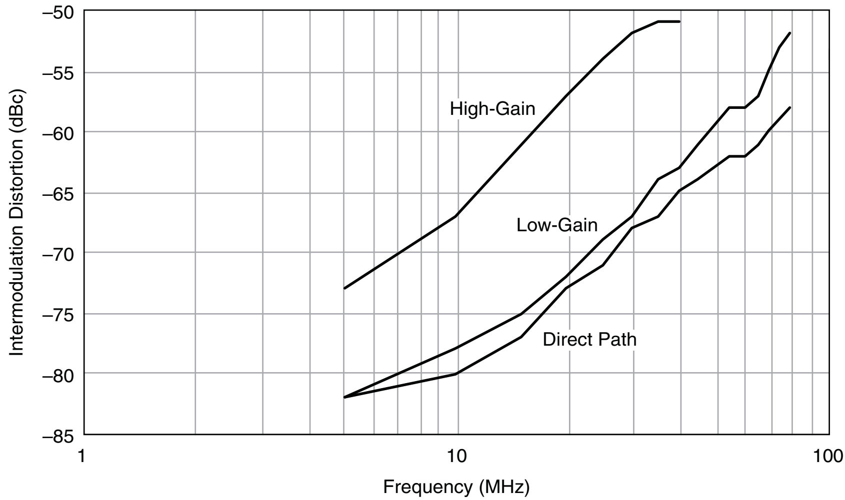
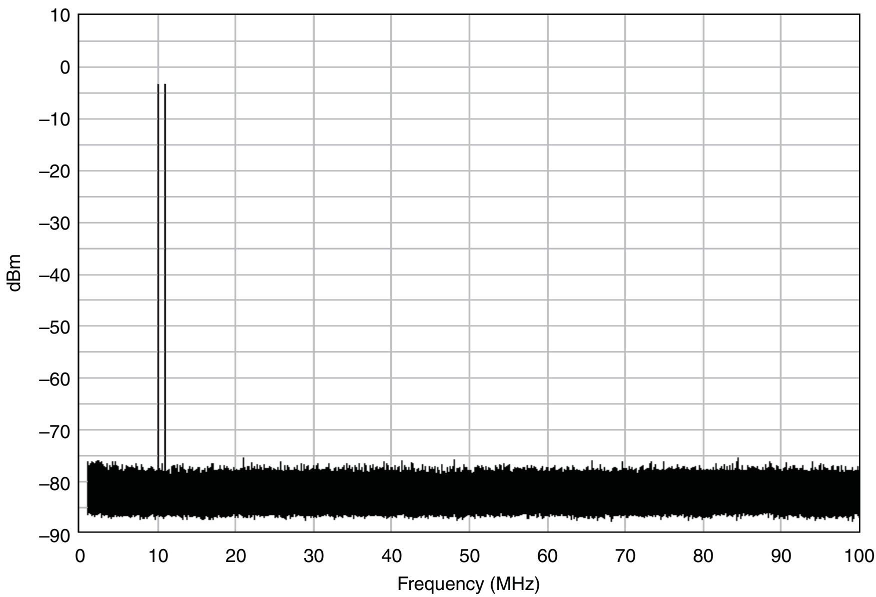


Figure 12. Direct Path, Two-Tone Spectrum (Typical)



Note The noise floor in Figure 12 is limited by the noise floor of the measurement device. Refer to the *Average Noise Density* specification for more information about this limit.

Sample Clock

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>Sources</td><td colspan="2">1. Internal, Divide-by-N (N ≥ 1)
2. Internal, DDS-based, High-Resolution
3. External, CLK IN (SMB front panel connector)
4. External, DDC CLK IN (DIGITAL DATA & CONTROL front panel connector)
5. External, PXI Star trigger (backplane connector)
6. External, PXI_Trig<0..7> (backplane connector)</td><td>Refer to the Onboard Clock (Internal VCXO) section for more information about internal clock sources.</td></tr>
<tr><td colspan="4">Sample Rate Range and Resolution</td></tr>
<tr><td>Sample Clock Source</td><td>Sample Rate Range</td><td>Sample Rate Resolution</td><td rowspan="7">—</td></tr>
<tr><td>Divide-by-N</td><td>5 to 200 MS/s</td><td>Settable to (200 MS/s)/N (1 ≤ N ≤ 40)</td></tr>
<tr><td>High Resolution</td><td>5 to 100 MS/s
>100 to 200 MS/s</td><td>1.06 µHz
4.24 µHz</td></tr>
<tr><td>CLK IN</td><td>5 to 200 MS/s</td><td rowspan="4">Resolution determined by external clock source.
External sample clock duty cycle tolerance 40 to 60%.</td></tr>
<tr><td>DDC CLK IN</td><td>5 to 200 MS/s</td></tr>
<tr><td>PXI Star Trigger</td><td>5 to 105 MS/s</td></tr>
<tr><td>PXI_Trig <0..7></td><td>5 to 20 MS/s</td></tr>
</table>

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td colspan="6">Sample Clock Delay Range and Resolution</td></tr>
<tr><td>Sample Clock Source</td><td colspan="3">Delay Adjustment Range</td><td>Delay Adjustment Resolution</td><td rowspan="5">—</td></tr>
<tr><td>Divide-by-N</td><td colspan="3">±1 sample clock period</td><td><5 ps</td></tr>
<tr><td>High-Resolution ≤100 MHz</td><td colspan="3">±1 sample clock period</td><td>sample clock period/16,384</td></tr>
<tr><td>High-Resolution >100 MHz</td><td colspan="3">±1 sample clock period</td><td>sample clock period/4,096</td></tr>
<tr><td>External (all)</td><td colspan="3">0 to 7.6 ns</td><td><15 ps</td></tr>
<tr><td colspan="6">System Phase Noise and Jitter (10 MHz Carrier)</td></tr>
<tr><td rowspan="2">Sample Clock Source</td><td colspan="3">System Phase Noise Density (dBc/Hz) Offset</td><td rowspan="2">System Output Jitter (Integrated from 100 Hz to 100 kHz)</td><td rowspan="7">Specified at 2× DAC oversampling. All values are typical.</td></tr>
<tr><td>100 Hz</td><td>1 kHz</td><td>10 kHz</td></tr>
<tr><td>Divide-by-N</td><td>-110</td><td>-122</td><td>-138</td><td>1.5 ps rms</td></tr>
<tr><td>High-Resolution* 100 MS/s</td><td>-109</td><td>-120</td><td>-120</td><td>4.0 ps rms</td></tr>
<tr><td>High-Resolution* 200 MS/s</td><td>-108</td><td>-120</td><td>-122</td><td>4.2 ps rms</td></tr>
<tr><td>CLK IN†</td><td>-116</td><td>-130</td><td>-143</td><td>1.1 ps rms</td></tr>
<tr><td>PXI Star Trigger†, ‡</td><td>-111</td><td>-128</td><td>-136</td><td>2.1 ps rms</td></tr>
<tr><td>External Sample Clock Input Jitter Tolerance</td><td colspan="4">Cycle-Cycle Jitter ±150 ps
Period Jitter ±1 ns</td><td>All values are typical.</td></tr>
<tr><td colspan="6">* High-Resolution specifications vary with Sample Rate.
† Values are typical.
‡ PXI Star trigger specification is valid when the sample clock source is locked to PXI_CLK10.</td></tr>
</table>

Specification	Value			Comments
Sample Clock Exporting				
Exported Sample Clock Destinations	1. PFI<0..1> (SMB front panel connectors) 2. DDC CLK OUT (DIGITAL DATA & CONTROL front panel connector) 3. PXI_Trig<0..6> (PXI backplane connector)			Exported sample clocks can be divided by integer K ($1 \leq K \leq$ 4,194,304).
Exported Sample Clock Destinations	Maximum Frequency	Jitter (Typical)	Duty Cycle	—
PFI<0..1>	200 MHz	PFI 0: 6 ps rms PFI 1: 12 ps rms	25 to 65%	
DDC CLK OUT	200 MHz	60 ps rms	35 to 65%	
PXI_Trig <0..6>	20 MHz	—	—	

Onboard Clock (Internal VCXO)

Specification	Value	Comments
Clock Source	Internal sample clocks can either be locked to a reference clock using a phase-locked loop or be derived from the onboard VCXO frequency reference.	—
Frequency Accuracy	±25 ppm	—

Phase-Locked Loop (PLL) Reference Clock

Specification	Value	Comments
Sources	1. PXI_CLK10 (backplane connector) 2. CLK IN (SMB front panel connector)	The PLL Reference Clock provides the reference frequency for the phase-locked loop.
Frequency Accuracy	When using the PLL, the frequency accuracy of the NI 5422 is solely dependent on the frequency accuracy of the PLL reference clock source.	—
Lock Time	≤200 ms	All values are typical.
Frequency Range	5 to 20 MHz in increments of 1 MHz.Default of 10 MHz The PLL reference clock frequency has to be accurate to ±50 ppm.	—
Duty Cycle Range	40 to 60%	—
Exported PLL Reference Clock Destinations	1. PFI<0..1> (SMB front panel connectors) 2. PXI_Trig<0..6> (backplane connector)	—

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Specification	Value	Comments
Connector	SMB (jack)	—
Direction	Input	—
Destinations	1. Sample Clock 2. PLL Reference Clock	—
Frequency Range	5 to 200 MHz (Sample Clock Destination) 5 to 20 MHz (PLL Reference Clock destination)	—

Specification	Value	Comments
Input Voltage Range	Sine wave: 0.65 to 2.8 Vpk-pk into 50 Ω (0 dBm to +13 dBm) Square wave: 0.2 to 2.8 Vpk-pk into 50 Ω	—
Maximum Input Overload	±10 V	—
Input Impedance	50 Ω	—
Input Coupling	AC	—

PFI 0 and PFI 1 (Programmable Function Interface, Front Panel Connectors)

Specification	Value	Comments
Connectors	Two SMB (jack)	—
Direction	Bidirectional	—
Frequency Range	DC to 200 MHz	—
As an Input (Trigger)		
Destinations	Start trigger	—
Maximum Input Overload	-2 to +7 V	—
V_{IH}	2.0 V	—
V_{IL}	0.8 V	—
Input Impedance	1 kΩ	—
As an Output (Event)		
Sources	1. Sample clock divided by integer K ($1 \le K \le 4{,}194{,}304$) 2. Sample clock timebase (200 MHz) divided by integer M ($4 \le M \le 4{,}194{,}304$) 3. PLL reference clock 4. Marker 5. Exported start trigger (Out Start Trigger)	—
Output Impedance	50 Ω	—

Specification	Value	Comments
As an Output (Continued)		
Maximum Output Overload	-2 to +7 V	—
V_{OH}	Minimum: 2.7 V (open load), 1.3 V (50 Ω load)	Output drivers are +3.3 V TTL compatible.
V_{OL}	Maximum: 0.6 V (open load), 0.2 V (50 Ω load)	
Rise/Fall Time (20 to 80%)	≤2.0 ns	Load of 10 pF.

Digital Data & Control (DDC) Optional Front Panel Connector

Specification	Value	Comments
Connector Type	68-pin VHDCI female receptacle	—
Number of Data Output Signals	16	—
Control Signals	1. DDC CLK OUT (clock output) 2. DDC CLK IN (clock input) 3. PFI 2 (input) 4. PFI 3 (input) 5. PFI 4 (output) 6. PFI 5 (output)	—
Ground	23 pins	—

Specification	Value			Comments
Output Signal Characteristics (Includes Data Outputs, DDC CLK OUT, and PFI<4..5>)				
Signal Type	LVDS (Low-Voltage Differential Signal)			—
Signal Characteristics	Minimum	Typical	Maximum	Tested with 100 Ω differential load. Measured with 188143B-01 cable. Driver and receiver comply with ANSI/TIA/EIA-644. All values are typical.
V_{OH}	—	1.3 V	1.7 V	
V_{OL}	0.8 V	1.0 V	—	
Differential Output Voltage	0.25 V	—	0.45 V	
Output Common-Mode Voltage	1.125 V	—	1.375 V	
Rise/Fall Time (20 to 80%)	—	0.8 ns	1.6 ns	
Output Signal Characteristics				
Output Skew	Typical: 1 ns, maximum 2 ns. Skew between any two outputs on the DIGITAL DATA & CONTROL front panel connector.			—
Output Enable/Disable	Controlled through the software on all Data Output Signals and Control Signals collectively. When disabled, the outputs go to a high-impedance state.			—
Maximum Output Overload	-0.3 to +3.9 V			—
Input Signal Characteristics (Includes DDC CLK IN and PFI<2..3>)				
Signal Type	LVDS (Low-Voltage Differential Signal)			—
Input Differential Impedance	100 Ω			—
Maximum Output Overload	-0.3 to +3.9 V			—

Specification	Value		Comments
Signal Characteristics	Minimum	Maximum	—
Differential Input Voltage	0.1 V	0.5 V	
Input Common Mode Voltage	0.2 V	2.2 V	
DDC CLK OUT			
Clocking Format	Data outputs and markers change on the falling edge of DDC CLK OUT.		—
Frequency Range	Refer to the *Sample Clock* section for more information.		—
Duty Cycle	35 to 65%		—
Jitter	60 ps rms (typical)		—
DDC CLK IN			
Clocking Format	DDC Data Output signals change on the rising edge of DDC CLK IN.		—
Frequency Range	10 Hz to 200 MHz		—
Input Duty Cycle Tolerance	40 to 60%		—

Start Trigger

Specification	Value	Comments
Sources	1. PFI<0..1> (SMB front panel connectors) 2. PFI<2..3> (DIGITAL DATA & CONTROL front panel connector) 3. PXI_Trig<0..7> (PXI backplane connector) 4. PXI Star trigger (PXI backplane connector) 5. Software (use function call) 6. Immediate (does not wait for a trigger). Default.	—
Modes	1. Single 2. Continuous 3. Stepped 4. Burst	—
Edge Detection	Rising	—
Minimum Pulse Width	25 ns	Refer to t_{s1} at **NI Signal Generators Help»Devices» NI 5422» Triggering» Trigger Timing**.
Delay from Start Trigger to CH 0 Analog Output	65 sample clock periods + 110 ns	Refer to t_{s2} at **NI Signal Generators Help»Devices» NI 5422» Triggering» Trigger Timing**. All values are typical.
Delay from Start Trigger to Digital Data Output	41 sample clock periods + 110 ns	—

Specification	Value	Comments
Trigger Exporting		
Exported Trigger Destinations	A signal used as a trigger can be routed out to any destination listed in the *Destinations* specification in the *Markers* section.	—
Exported Trigger Delay	65 ns (typical).	Refer to t_{s3} at **NI Signal Generators Help»Devices» NI 5422» Triggering» Trigger Timing**.
Exported Trigger Pulse Width	>150 ns	Refer to t_{s4} at **NI Signal Generators Help»Devices» NI 5422» Triggering» Trigger Timing**.

Markers

Specification	Value	Comments
Destinations	1. PFI<0..1> (SMB front panel connectors) 2. PFI<4..5> (DIGITAL DATA & CONTROL front panel connector) 3. PXI_Trig<0..6> (backplane connector)	—
Quantity	One marker per segment.	—
Quantum	Marker position must be placed at an integer multiple of four samples.	—

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>Width</td><td colspan="3">>150 ns</td><td>Refer to t_{m2} at NI Signal Generators Help» Fundamentals» Waveform» Events» Marker Events.</td></tr>
<tr><td rowspan="4">Skew</td><td>Destination</td><td>With Respect to Analog Output</td><td>With Respect to Digital Data Output</td><td rowspan="4">Refer to tm1 at NI Signal Generators Help» Fundamentals» Waveform» Events» Marker Events.</td></tr>
<tr><td>PFI<0..1></td><td>±2 sample clock periods</td><td>N/A</td></tr>
<tr><td>PFI<4..5></td><td>N/A</td><td><2 ns</td></tr>
<tr><td>PXI_Trig <0..6></td><td>±2 sample clock periods</td><td>N/A</td></tr>
<tr><td>Jitter</td><td colspan="3">40 ps rms (typical)</td><td>—</td></tr>
</table>

Arbitrary Waveform Generation Mode

Specification	Value	Comments
Memory Usage	The NI 5422 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.	—
Onboard Memory Size	8 MB standard: 8,388,608 bytes 256 MB option: 268,435,456 bytes 32 MB option: 33,554,432 bytes 512 MB option: 536,870,912 bytes	—
Output Modes	Arbitrary Waveform mode and Arbitrary Sequence mode	—
Arbitrary Waveform Mode	In Arbitrary Waveform mode, a single waveform is selected from the set of waveforms stored in onboard memory and generated.	—

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td>Arbitrary Sequence Mode</td><td colspan="4">In Arbitrary Sequence mode, a sequence directs the NI 5422 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as segments. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which sample in the waveform a marker output signal is sent.</td><td>—</td></tr>
<tr><td rowspan="8">Minimum Waveform Size (Samples)</td><td>Trigger Mode</td><td>Arbitrary Waveform Mode</td><td colspan="2">Arbitrary Sequence Mode</td><td rowspan="8">The minimum waveform size is sample rate dependent in Arbitrary Sequence mode.</td></tr>
<tr><td>Single</td><td>16</td><td colspan="2">16</td></tr>
<tr><td rowspan="2">Continuous</td><td rowspan="2">32</td><td colspan="2">192 at >50 MS/s</td></tr>
<tr><td colspan="2">96 at ≤50 MS/s</td></tr>
<tr><td rowspan="2">Stepped</td><td rowspan="2">32</td><td colspan="2">192 at >50 MS/s</td></tr>
<tr><td colspan="2">96 at ≤50 MS/s</td></tr>
<tr><td rowspan="2">Burst</td><td rowspan="2">32</td><td colspan="2">192 at >50 MS/s</td></tr>
<tr><td colspan="2">96 at ≤50 MS/s</td></tr>
<tr><td>Loop Count</td><td colspan="4">1 to 16,777,215
Burst trigger: Unlimited</td><td>—</td></tr>
<tr><td>Quantum</td><td colspan="4">Waveform size must be an integer multiple of four samples</td><td>—</td></tr>
<tr><td colspan="6">Memory Limits</td></tr>
<tr><td></td><td>8 MB Standard</td><td>32 MB Option</td><td>256 MB Option</td><td>512 MB Option</td><td rowspan="2">All trigger modes except where noted.</td></tr>
<tr><td>Arbitrary Waveform Mode, Maximum Waveform Memory</td><td>4,194,176 samples</td><td>16,777,088 samples</td><td>134,217,600 samples</td><td>268,435,328 samples</td></tr>
<tr><td>Arbitrary Sequence Mode, Maximum Waveform Memory</td><td>4,194,048 samples</td><td>16,776,960 samples</td><td>134,217,472 samples</td><td>268,435,200 samples</td><td>Condition: One or two segments in a sequence.</td></tr>
</table>

Specification	Value				Comments
Arbitrary Sequence Mode, Maximum Waveforms	65,000 Burst trigger: 8,000	262,000 Burst trigger: 32,000	2,097,000 Burst trigger: 262,000	4,194,000 Burst trigger: 524,000	Condition: One or two segments in a sequence.
Arbitrary Sequence Mode, Maximum Segments in a Sequence	104,000 Burst trigger: 65,000	418,000 Burst trigger: 262,000	3,354,000 Burst trigger: 2,090,000	6,708,000 Burst trigger: 4,180,000	Condition: Waveform memory is <4,000 samples.

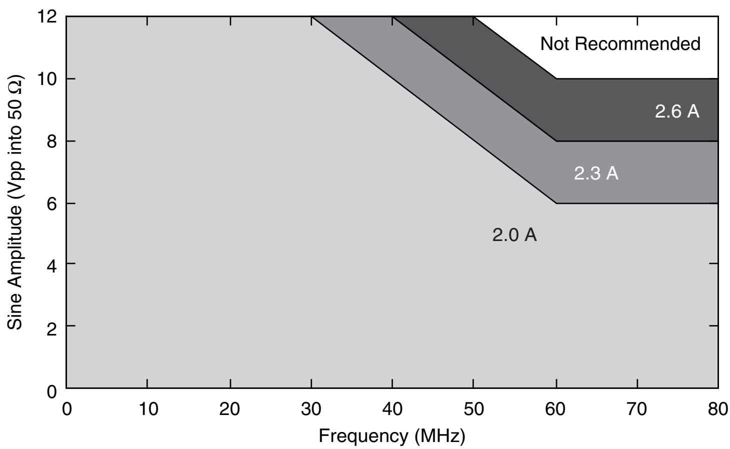
Calibration

Specification	Value	Comments
Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 90 seconds to complete.	—
External Calibration	The external calibration calibrates the VCXO, voltage reference, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.	—
Calibration Interval	Specifications valid within two years of external calibration.	—
Warm-up Time	15 minutes	—

Power

Specification	Typical Operation	Overload Operation	Comments
+3.3 VDC	2 A	2 A	Typical Operation is sine output, with analog filter, 50 Ω termination. 200 MS/s High-Resolution sample clock. Digital Pattern enabled and terminated, sample clock routed to PFI 0 and terminated. Overload operation occurs when CH 0 is shorted to ground.
+5 VDC	Refer to Figure 13	2.7 A	
+12 VDC	0.46 A	0.46 A	
-12 VDC	0.01 A	0.01 A	
Total Power	12.2 W + 5 V × 5 V Current	25.7 W	

Figure 13. 5 V Current Versus Frequency and Amplitude



Software

Specification	Value	Comments
Driver Software	NI-FGEN is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5422. NI-FGEN provides application programming interfaces for many development environments.	—
Application Software	NI-FGEN provides programming interfaces for the following application development environments: • LabVIEW • LabWindows™/CVI™ • Measurement Studio • Microsoft Visual C++ .NET • Microsoft Visual C/C++ • Microsoft Visual Basic	—
Interactive Control and Configuration software	The FGEN Soft Front Panel supports interactive control of the NI 5422. The FGEN Soft Front Panel is included on the NI-FGEN driver CDs. Measurement & Automation Explorer (MAX) provides interactive configuration and test tools for the NI 5422. MAX is also included on the NI-FGEN CDs. You can use the NI 5422 with NI SignalExpress.	—

Physical

Specification	Value	Comments
Dimensions	3U, One Slot, PXI/cPCI Module 21.6 × 2.0 × 13.0 cm (8.5 × 0.8 × 5.1 in.)	—
Weight	352 g (12.4 oz)	—

Specification	Value		Comments
Front Panel Connectors			
Label	Function(s)	Connector Type	—
CH 0	Analog Output	SMB (jack)	
CLK IN	Sample clock input and PLL reference clock input.	SMB (jack)	
PFI 0	Marker output, trigger input, sample clock output, exported trigger output, and PLL reference clock output.	SMB (jack)	
PFI 1	Marker output, trigger input, sample clock output, exported trigger output, and PLL reference clock output.	SMB (jack)	
DIGITAL DATA & CONTROL	Digital data output, trigger input, exported trigger output, markers, external sample clock input, and sample clock output.	68-pin VHDCI female receptacle	
Front Panel LED Indicators			
Label	Function		For more information, refer to the *NI Signal Generators Help*.
ACCESS	The ACCESS LED indicates the status of the PCI bus and the interface from the NI 5422 to the controller.		
ACTIVE	The ACTIVE LED indicates the status of the onboard generation hardware of the NI 5422.		
Included Cable			
—	1 (NI part number 763541-01), 50 Ω, BNC Male to SMB Plug, RG223/U, Double Shielded, 1 m cable.		—

Note NI PXI-5422 modules of revision B or later are equipped with a modified PXI Express-compatible backplane connector. This modified connector allows the NI PXI-5422 to be supported by hybrid slots in a PXI Express chassis. To determine the revision of an NI PXI-5422 module, read the label on the underside of the

NI PXI-5422. The label will list an assembly number of the format 191946x-01, where *x* is the revision.

Environment

NI PXI-5422 Environment

Note To ensure that the NI PXI-5422 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5422 kit.

Specifications	Value	Comments
Operating Temperature	0 to +55 ºC in all NI PXI chassis except the following: 0 to +45 ºC when installed in an NI PXI-101*x* or NI PXI-1000B chassis. (Meets IEC 60068-2-1 and IEC 60068-2-2.)	—
Storage Temperature	-25 to +85 ºC. Meets IEC 60068-2-1 and IEC 60068-2-2.	—
Operating Relative Humidity	10 to 90%, noncondensing. Meets IEC 60068-2-56.	—
Storage Relative Humidity	5 to 95%, noncondensing. Meets IEC 60068-2-56.	—
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	Spectral and jitter specifications could degrade.
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Operating Vibration	5 to 500 Hz, 0.31 $g_{rms.}$ Meets IEC 60068-2-64.	Spectral and jitter specifications could degrade.
Storage Vibration	5 to 500 Hz, 2.46 g_{rms}. Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 m maximum (at 25 °C ambient temperature)	—

Specifications	Value	Comments
Pollution Degree	2	—
Indoor use only.		

Compliance and Certifications

Safety

The NI PXI-5422 is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label, or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility (EMC)

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions, Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

CE Compliance

The NI PXI-5422 meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Online Product Certification

To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

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Visit ni.com/services for NI Factory Installation Services, repairs, extended warranty, and other services.

Visit ni.com/register to register your National Instruments product. Product registration facilitates technical support and ensures that you receive important information updates from NI.

A Declaration of Conformity (DoC) is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification. If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

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