Domain-Specific Processor Design using ASIP Designer

The RISC-V initiative has raised increased awareness about the design of domain-specific or application-specific processors, which implement a specialized instruction set architecture (ISA), often starting from a baseline ISA such as RISC-V.

But designers are faced with the challenges of determining the best ISA for their specific application, how to get to a compiler and a simulator for the specialized architecture, and how to know if the target performance can be reached.

Synopsys ASIP Designer is a design tool that automates the design of application-specific processors. Starting from a single processor specification that allows to model standard ISAs such as RISC-V as well as any kind of specializations, designers get a cycle-accurate simulator, debugger and an optimizing C/C++ Compiler, all supporting the specialized ISA. This allows for a compiler-in-the-loop based tuning of the processor specification, using the real application code to benchmark the performance. From the same specification, the RTL code is generated, which allows to measure the gate count and to identify critical paths in the design.

Top semiconductor and systems companies worldwide deploy ASIP Designer for innovative designs on aggressive schedules with limited design teams.

ASIP Designer is available to CNDN member Universities in Canada through CMC Microsystem.

Join us for this series of training sessions, to learn more about ASIP Designer, and how you may use it for your next project.

Session 1: ASIP Designer Tool and Methodology Training

August 25th, 10:00 am – 14:30 pm

- What you will learn:
    - Introduction to ASIP Designer: look and feel
    - Introduction to the ASIP design methodology, which allows for a profiling-driven optimization of the processor architecture
    - Introduction to the Hands-on exercise: Designing an ASIP specialized for SHA-256 acceleration, extending a RISC-V processor.

August 26th: Students will get access to the necessary tool licenses to do the hands-on lab at their own pace. Questions can be submitted to instructors via email.

Session 2: ASIP Designer, Example Models

August 27th, 10:00 am – 12:00 pm

- What you will learn:
    - ASIP Designer comes with a wide range of example models. These models are provided in source code so they can be easily modified to serve both as a starting point for a customer design, as well as a reference how to model certain architectural features.

- During this session we will give an overview of the models available, and will do a deep-dive into a number of models, ranging from microcontrollers such as RISC-V to VLIW-models all the way to highly specialized yet fully programmable accelerators

Session 3: ASIP Designer Q&A session
August 27th, 12:45 pm – 14:15 pm

- This session is intended to be interactive. If you have been using ASIP Designer already, you may came across questions that were not covered by the manuals. This is the forum to bring them up, with Synopsys application engineers available to address them