Community consultation about heterogeneous integration

OCTOBER 25, 2019 | ANDREW FUNG

CMC MICROSYSTEMS

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Webinar agenda

- (moderator) Andrew Fung, CMC Microsystems
  Group Lead, Microelectronics and MEMS
- Introduction to CMC Microsystems
- Heterogeneous Integration Roadmap: Integrated Photonics (Prof. Amr Helmy, U. Toronto and member of International Roadmap Committee)
- 2.5D Multi-Technology Silicon Interposer Platform (Gordon Harling, President and CEO, CMC Microsystems)
- Q&A, community feedback

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What is CMC and its role?

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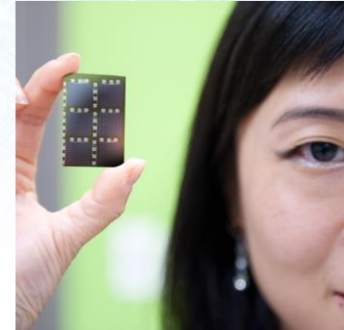
CMC Microsystems

- CMC provides services essential for the research and training required to advance Canada's digital economy:
  - Industry 4.0, autonomous vehicles, big data, Internet of Things (IoT), cyber defence and security, 5G, quantum computing, artificial intelligence (AI),
and more!



- Academic and Industrial Users
  - Not-for-profit founded in 1984
  - Manages Canada's National Design Network®
  - Delivers micro-nano innovation capabilities
across Canada

CMC

Lowering barriers to technology adoption

CAD

State-of-the-art environments for successful design

- Selection of high-performance Computer Aided Design (CAD) tools and design environments
- Available via desktop or through CMC Cloud
- User guides, application notes, training materials and courses

FAB

Services for making working prototypes

- Multi-project wafer services with affordable access to foundries worldwide
- Fabrication and travel assistance to prototype at a university-based lab
- Value-added packaging and assembly services
- In-house expertise for first-time-right prototypes

LAB

Device validation to system demonstration

- Access to platform-based microsystems design and prototyping environments
- Access to test equipment on loan
- Access to contract engineering services

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Heterogeneous Integration Roadmap: Integrated Photonics

Prof. Amr Helmy, U. Toronto
Member of IEEE HIR International Roadmap Committee

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- For presentations about the IEEE Heterogeneous Integration Roadmap, visit
- https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

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2.5D Multi-Technology Silicon Interposer Platform

Gordon Harling, President and CEO, CMC Microsystems

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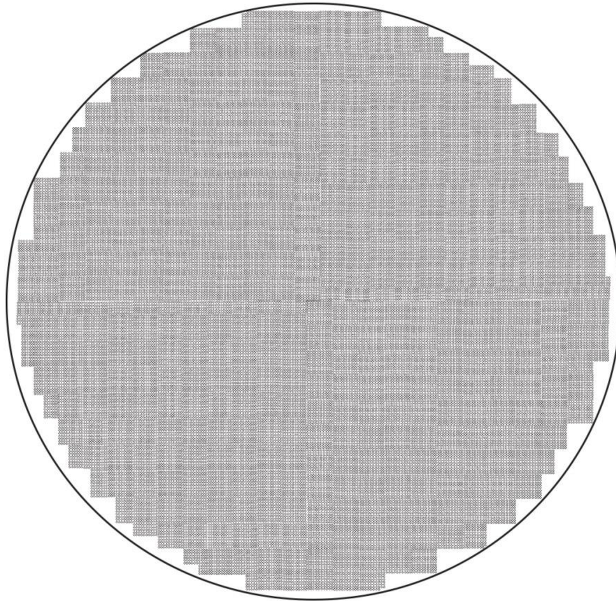
What we are doing

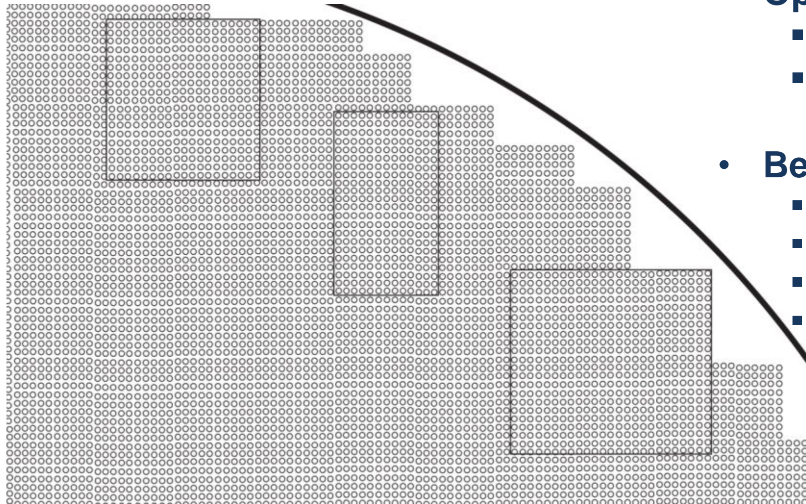
Silicon interposer – Wafer view



- **<u>Method</u>:**
- **We start-off with an 8" wafer**
- **Pattern (array) TSVs uniformly across whole wafer**
- **No scribes or free area**
- **Removes limits to design size**
- **Standard tiles or custom arrays**

What we are doing

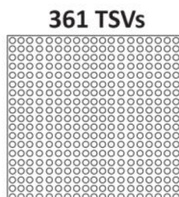
Silicon interposer – Custom sizes

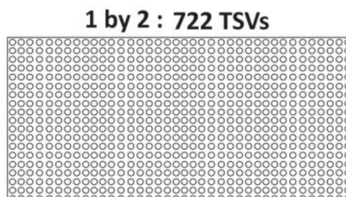


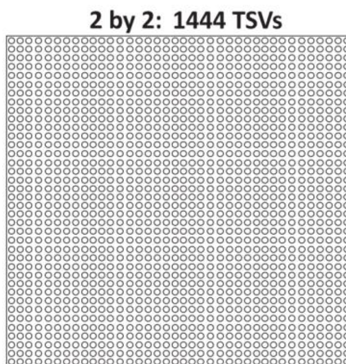
- Options:
  - Custom sizes
  - Quarter wafer / Full Wafer
- Benefits:
  - Larger designs possible
  - Short cycle time
  - TSV wafer inventory
  - Flexibility in size/shape/RDL

What we are doing for packaging?

Silicon interposer – Standard Tiles





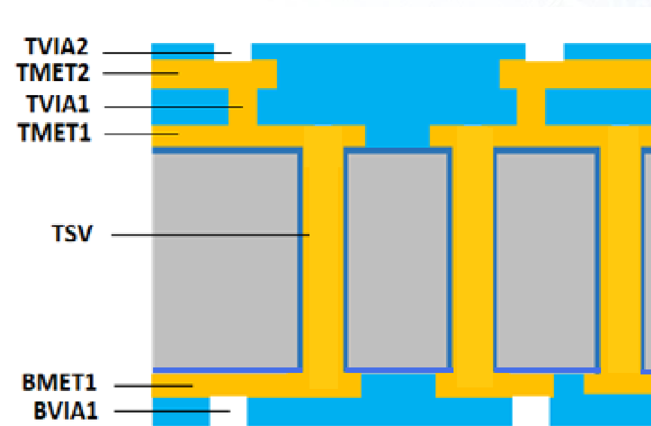


- **Options:**
  - **Base array 1 cm2: 19x19 TSVs**
  - **1x2 array: 19x38 TSVs**
  - **2x2 array: 38x38 TSVs**
- **Benefits:**
  - **Inventoried**
  - **Reduced cycle time 4-6 weeks for prototyping your design**
  - **Access to Test Sockets**

What we are doing

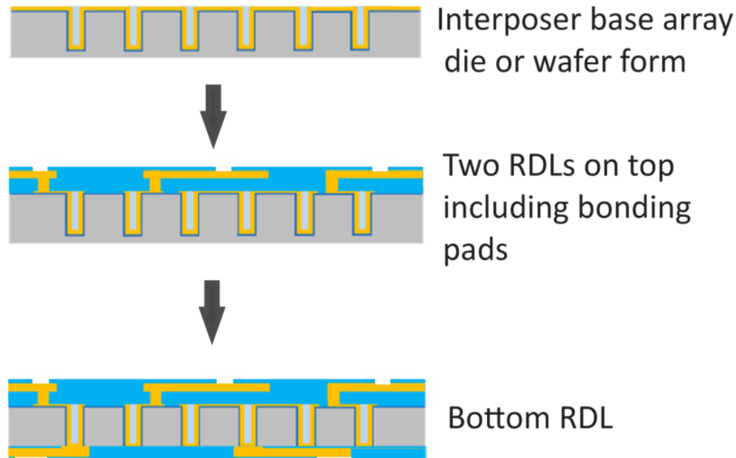
- <u>Very small sizes:</u>
- 400µm thickness
- 2 top RDL
- 1 bottom RDL
- 5µm metal width / spacing
- TSV diameter: 100µm
- TSV pitch: 500µm
- $\frac{1}{15}$ $Width_{PCB\ metal}$
- $\frac{1}{2}$ $thick_{bare\ die}$

Silicon interposer – Cross-sectional view



What we are doing

Silicon interposer – Flexible manufacturing



Four process modules:

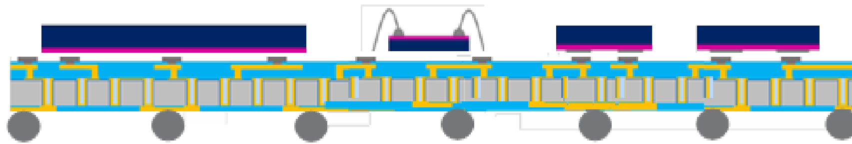
1. TSV Array formation
2. Top-side patterning
3. Bottom-side patterning
4. Component placement

Modular approach:

- Wafer hand-off mirrored
- Finished product
- Intercept manufacturing flow outside of validated network

What we are doing

Silicon interposer – Component placement



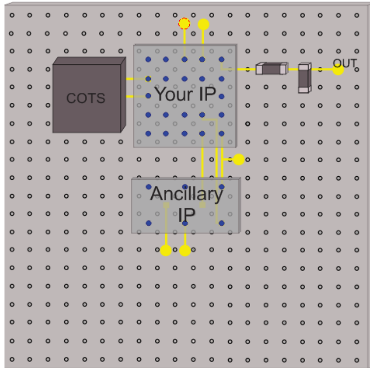
Preferred method Flip-chip → Also: Wirebonding

Process step 4:

- Ball drop bumping
- Stencil print
- Solder bumping
- Standard BGA: 100µm diameter 1mm pitch
- Underfill

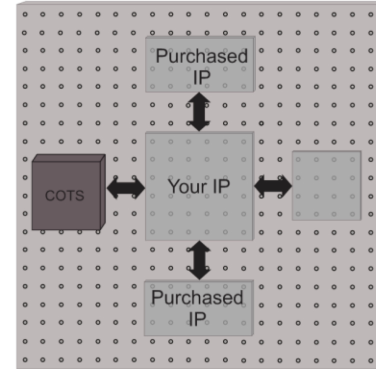
Why use the interposer

FLEXIBLE PROTO – IP Vendors



- Requirements vs Offer
- Variable demo for customer
- Customer: HW Eval, SW
- Close to final product: Speed, Size, Power

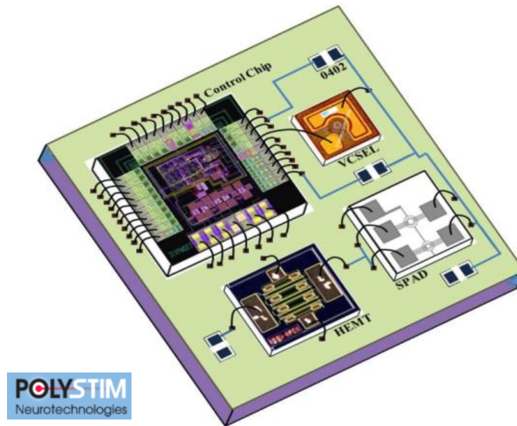
RAPID DEMO – SoC Developers



- Close to final IC: Speed, Power, Size
- De-risk of design
- 4-6 weeks turnaround time
- Early software development

Why use the interposer

FEASIBILITY – PROOF OF CONCEPT



On Chip Near InfraRed spectroscopy:
Portable brain imaging, Optical mammography

Benefits:

- Low-cost method
  - Demo
  - PoC
- Sellable form
- Increased capability: Speed, Size, Power
- Hiding complexity

- Excellent CTE
- No Outgassing
- Small Size, Portability

Why use the interposer?

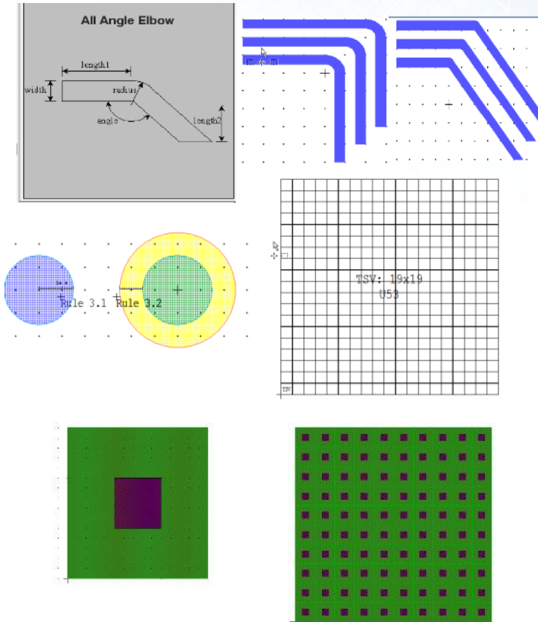
	PCB	Interposer
Line width	75 µm (3 mils)	5 µm (0.2 mil)
Line spacing	75 µm	5 µm
Line thickness	30 µm	1 µm
Relative Dielectric Const.	4.3	4
Loss tangent	0.025	0.0015
Spacing between layers	165 µm	1.5 µm
Wiring density	130 lines / cm sq.	600 lines / cm sq.

- Eliminate outgassing for pump down
- Wide temperature range

How we do it

Process Design Kit (PDK)

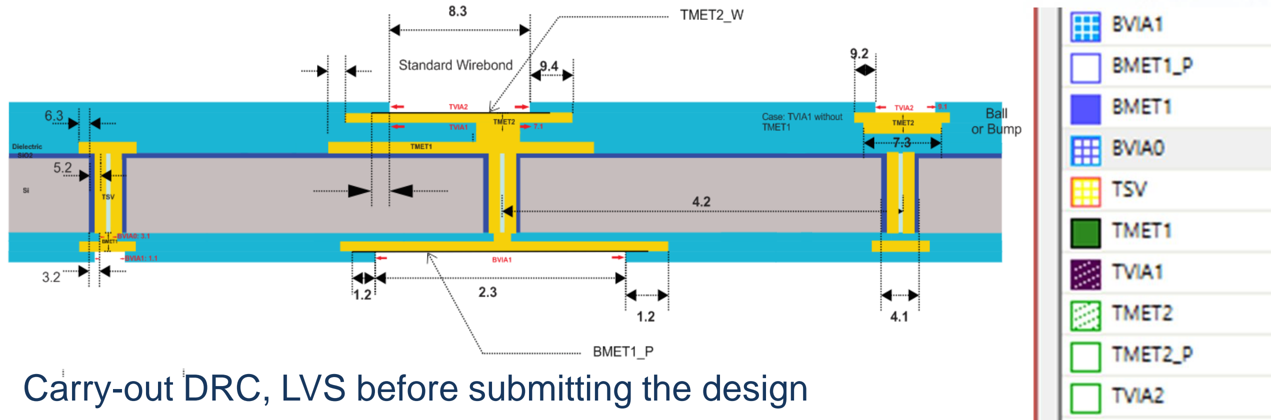
- Tanner Tools V2016 currently deployed
  - Curve tools add-on by softMEMS with G-S-G RF trace capability
  - Primitives, Cells for Pads, Contacts, TSV arrays and TSV connections
- Design rules always up to date
- Library of standard components
- Common surface mount and WLCSP footprints



How we do it

Process Design Kit (PDK)

- DRC Rules in User’s Guide

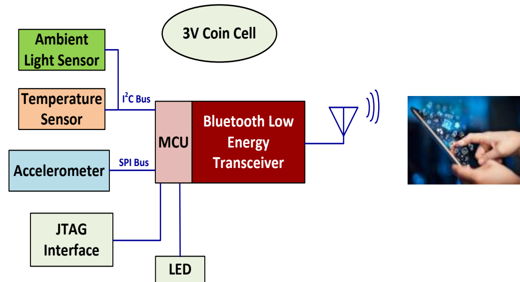


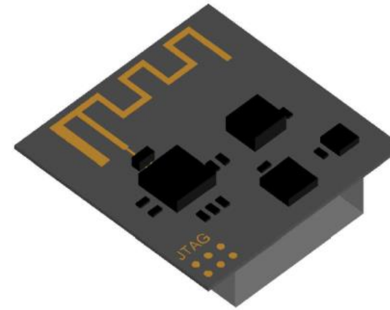
- Carry-out DRC, LVS before submitting the design
- Migrate your PCB designs

How we do it

Reference design 1 – Reusable IP – Crowdsourcing approach

Compact BLE sensor node



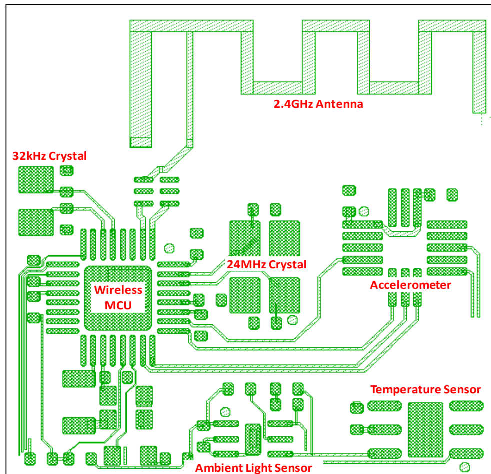


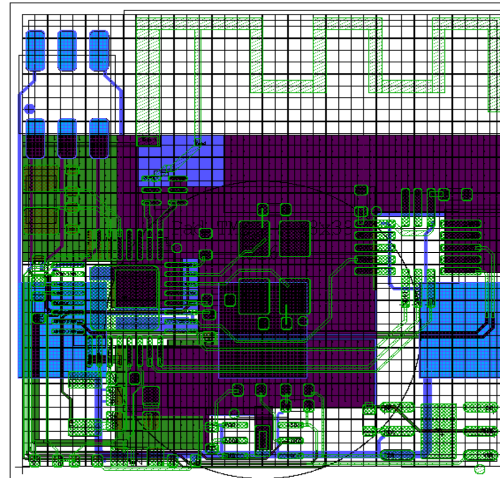
- Light, temp sensors, accelerometer, CC2640 MCU, coin cell
- Antenna incorporated on silicon interposer!
- Sharing common blocks of circuitry with users
- Library of schematics, layouts

How we do it

Reference design 1 – Reusable IP – Crowdsourcing approach

Compact BLE sensor node

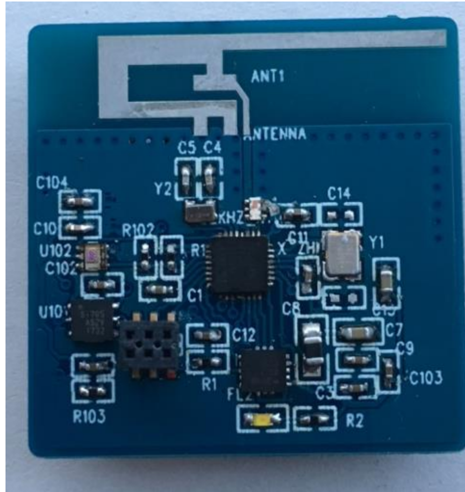




BVIA1
BMET1_P
BMET1
BVIA0
TSV
TMET1
TVIA1
TMET2
TMET2_P
TVIA2

Current status

Reference Design 1 – BLE Sensor

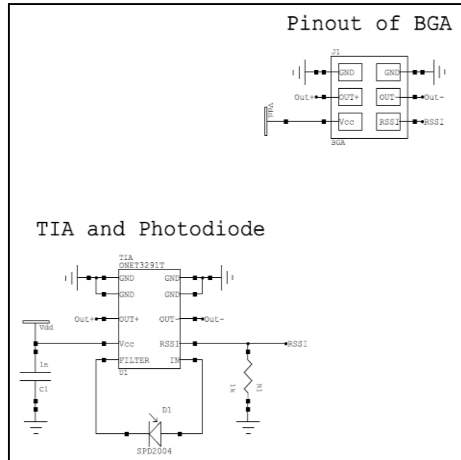


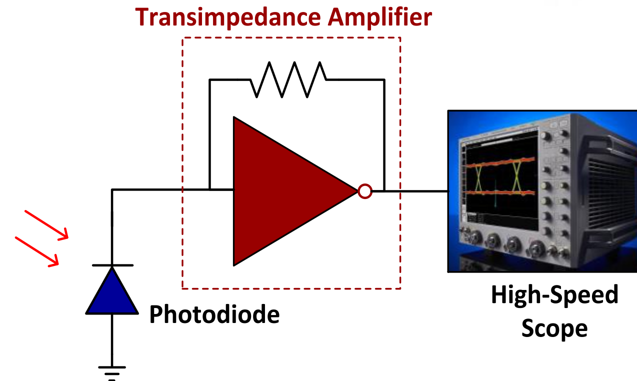
- Early PCB Version for FW Eval
- Published FW and Android App in December 2017
- Interposer version with integrated antenna (over TSVs) in design
- CMC plans on making FW available and modifiable for user's needs

How we do it

Reference design 2 – Reusable IP – Crowdsourcing approach

Optical receiver front-end

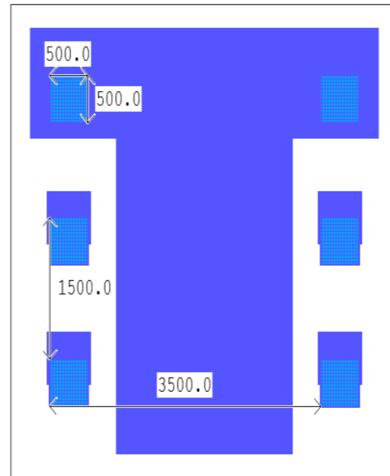


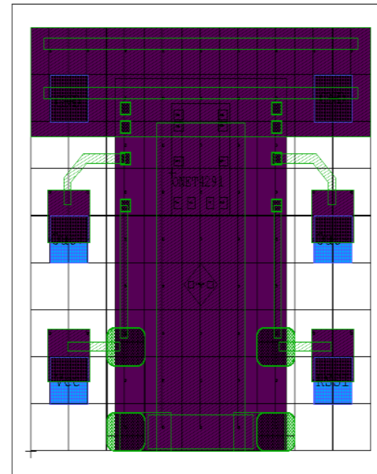


How we do it

Reference design 2 – Reusable IP – Crowdsourcing approach

Optical receiver front-end





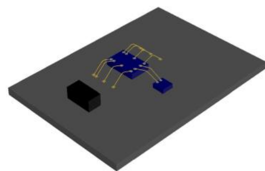
- BVIA1
- BMET1_P
- BMET1
- BVIA0
- TSV
- TMET1
- TVIA1
- TMET2
- TMET2_P
- TVIA2

How we do it

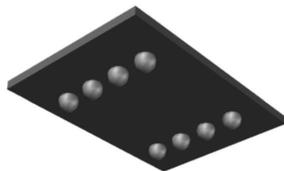
Reference design 2 – Reusable IP – Crowdsourcing approach

Optical receiver front-end

TOP VIEW



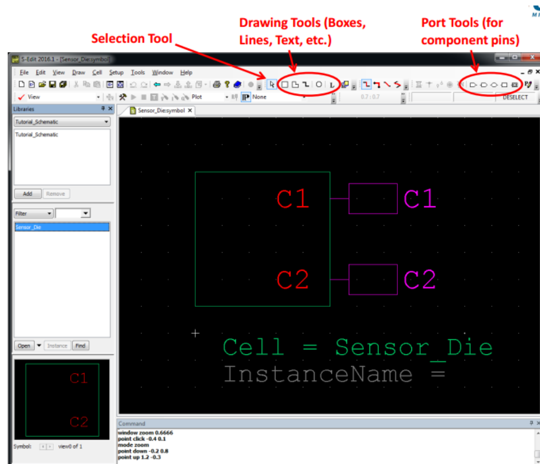
BOTTOM VIEW

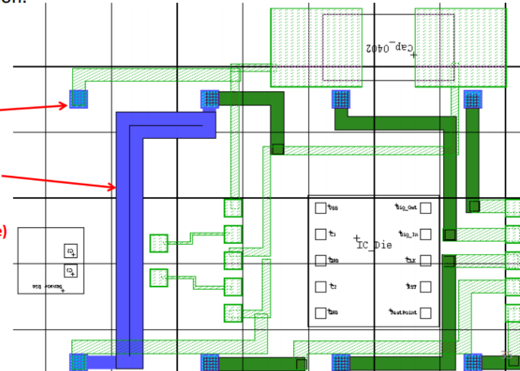


How we do it

Tanner Toolkit Features

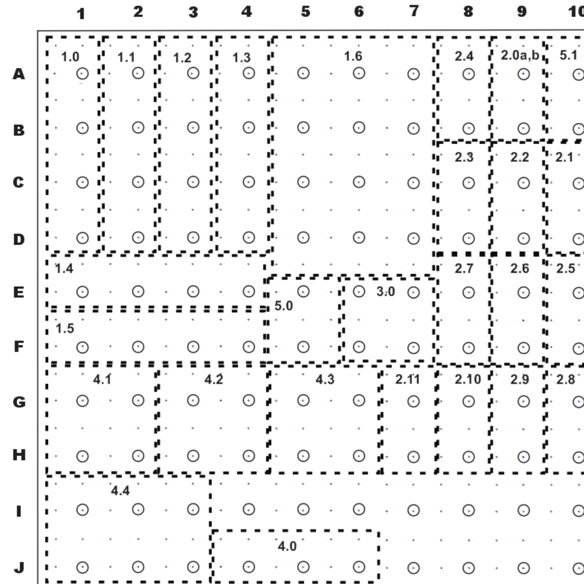
Fully downloadable User's Guides, Training Kits, Rules Decks and Design Tutorials





How we do it

Test Chip – Process Control Module (PCM)



Tests:

4-point resistance,

Contact chain,

Max current,

Continuity and Isolation,

S-Params on G-S-G

Test chip:

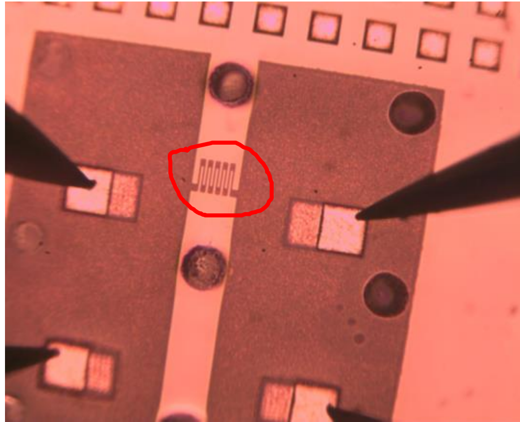
- Each supplier fabricates a PCM
- Choosing supplier according to test chip results

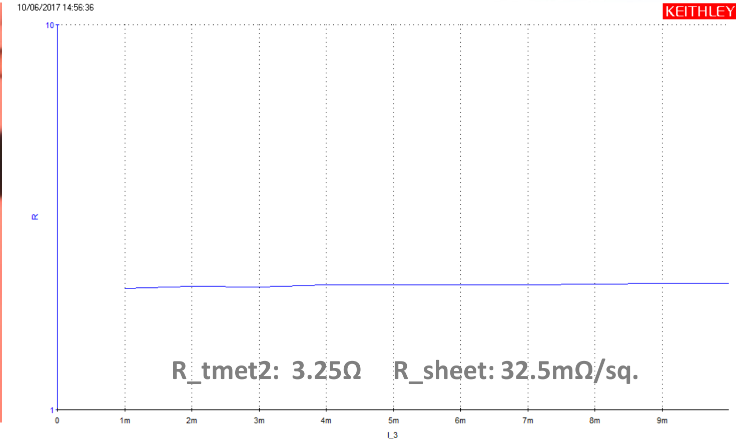
Suppliers:

- Design interception
- Skill sets, Equipment, Nature of design

How we do it

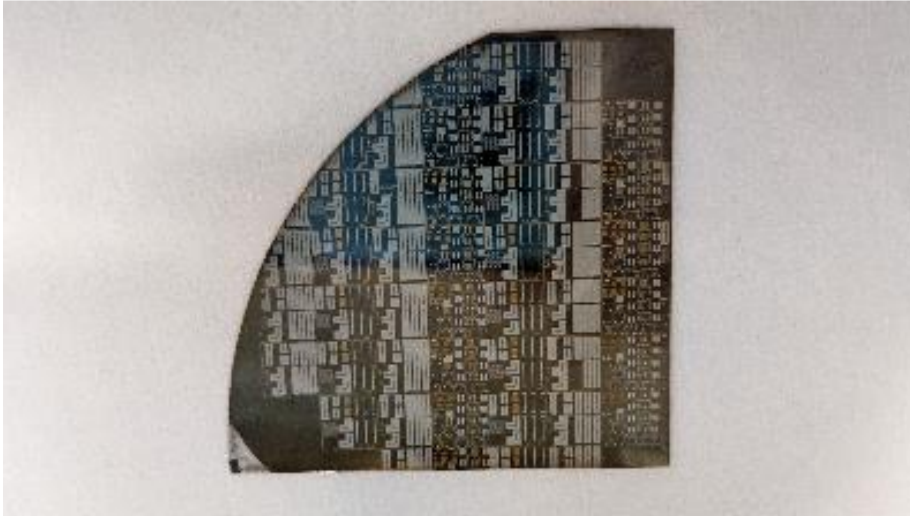
PCM – 4pt resistance





Follows: TMET1, BMET1, Contact chain, Max current, C&I

Current status



- PDK and tools ready
- New TSV process in development
- First runs of PCMs in 2020 for characterization

Community feedback

- What would help advance your technology R&D?
- What are your requirements for integration and packaging?
- Engage with CMC to develop platform technology.
- Other Q&A

- **Contact:**
- andrew.fung@cmc.ca fab@cmc.ca

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Coming up: NANOvember in Edmonton