Title: Neural Network for EDA Routability-driven Global Routing

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Abstract
Routing connecting wires for complex systems on chip (SoCs) presents formidable computational challenges and represents one of the most challenging problems in the so-called back-end physical design of SoCs (integrated circuits). Ensuing congestion, a key factor of routability, typically increases the number of vias and detours in the layout, and this generally negatively affects the overall circuit performance. Furthermore, congested areas in the layout may result in the creation of shorts and opens in the interconnect, negatively affecting the manufacturing yield or reliability of SoCs.

The traditional approaches employ algorithms to generate fixed models for congestion estimation which do not scale as the technology nodes scale to finer dimensions. We explore and develop an image-reconstruction regression neural network which makes congestion image predictions based on circuit layout properties. Furthermore, to solve the format compatibility issue caused by different EDA tools when generating input features, a “bridge” algorithm is developed which constructs universal feature images free from the choice of tools. We achieve comparable global routing quality, resulting in an average of more than 20% lower initial overflow counts. This initial quality improvement carries through to the final routing solution, with other estimation techniques needing up to 5% more routing iterations and at least 3x faster, in total, in routing all benchmarks.

Bio (Andre)
André Ivanov, is Professor of Electrical and Computer Engineering at UBC. He has published widely on many research topics related to the design and test of Systems on Chip (SoCs), and is an inventor of several patents. He is a Golden Core Member of the Computer Society, a Fellow of the IEEE, a Fellow of the Canadian Academy of Engineering, a Fellow of the Engineering Institute of Canada, and a Professional Engineer of British Columbia. Dr. Ivanov's current research interests are focused on new solutions and methodologies aimed at addressing reliability issues arising in SoCs in Internet of Things (IoT) applications. These methodologies include molecular dynamics simulations combined with machine learning approaches. Dr. Ivanov is also pursuing research in machine learning applications to electronic design automation (EDA) of SoCs.

Bio (Sebastian)
Zhonghua (Sebastian) Zhou is a Ph.D. candidate in the Department of Electrical and Computer Engineering at the University of British Columbia, Canada. He has had one and a half years of EDA industrial working experience at an EDA start-up company and at Synopsys. His doctoral research investigates the optimization of System on Chip (SoC) global routing techniques, the current project is focused on developing routability-driven routing strategies, which includes deep learning based congestion estimations, and congestion-aware routing algorithm.