## **Microsystems Technology Roadmap Overview**

## Canada's National Design Network, June 2018

	NDN Technology Cross	Year 1	Year 2	Year 3		Year 4	Year 5
	NDN Technology Space	2018	2019	2020		2021	2022
			Power-efficient embedded machine le				
	Embedded System and Machine Learning		☆Application-oriented training dataset	☆Multi-die-based heter			☆Memrister-based FPGA
SYSTEMS,		✓ Neural network co		dware/software AI platforn			
ARCHI-			<ul> <li>OpenCL for embedded FPGA/GPU</li> </ul>		euromorphic co-processor		
TECTURES, NETWORKS	Demonstrators		☆ASIP for Machine Learning	<ul> <li>High Bandwidth Memory</li> </ul>	, .		onnect processing node
	Demonstrators		☆AI edge/cloud demonstrator			🕸 Real-time heter	rogeneous operating system
		✓ Heterogeneous clo		Secure edge/cloud demonstrator			A Quantum Co-processor
		☆ KGD/CSP embedded processing library ✓ New flavors: SiGe: Imaging(CIS), LP • CMOS integrated Non-Volatile Memory • RF MEMS for optical communications					
	Microelectronics, MEMS/NEMS	V New Havors: Sige	⇒ 22nm SOI	,	30nm SiGe with Opto	<ul> <li>GAA/Nanowires</li> </ul>	
		✓ FinFET Simulation			ion von Neumann architecture		5 
		V FILLET SITUATION	Package PDK (Ad		Photonics and Microelectronics		
			· Fackage FDR (Au	Graphene coatings	notonics and whereeet onics	co-design now	<ul> <li>Heat dissipation (microfluidics)</li> </ul>
	11121113/1121113		St Cryogenic CMO	0	nd processes for 2.5D Heteroge	enous Integration	Cryogenic Memory
				ost processing (integration/		chous megration	e er jogene menner j
		🕸 MEMS pressure se		<ul> <li>THz communication (s</li> </ul>		enabled MEMS	<ul> <li>Low actuation voltage devices</li> </ul>
				1			
	Photonics: Silicon- Photonics, Ill-V, Optics	<ul> <li>SOI optimized for long wavelength</li> </ul>	☆ Monolithic phot	onic/microelectronic PDK			
		🕸 Hybrid SOI and Si3N4 platform	☆ Si-P PIC LVS with thermo-mechanical	modeling ☆	SV in Si-P MPW		<ul> <li>Intra-chip optical interconnect</li> </ul>
		☆ III-V integration pl	<ul> <li>Photonic device p</li> </ul>	oackage PDK • B	IST, ATPG for photonics		
DEVICES,		<ul> <li>Experimentally verified compact models</li> </ul>			ntegrated schematic-driven Si-	P and uE PDK	☆ Epi-based III-V gain block in SOI PDK
CIRCUITS,		<ul> <li>Integrated Si-P CAD tools with IP libraries</li> </ul>		✓ Integrated package /	chip PDK • Si-P in "zero	o change" CMOS	
TOPOLOGIES, SUBSYSTEMS		<ul> <li>e-beam prototyping</li> </ul>	🕸 Sub-wavelength				
		🕸 SOI on 300 mm w	afers		Photonics & Microelectronics c		
		☆ III-V bonded to Si		-	cladding for longer wavelength	h applications (8-10µm)	
		✓ Schematic-driven Si-Photonics design flow		<ul> <li>Strained Ge for direct</li> </ul>	gap applications		
		<ul> <li>Si3N4 for low loss and/or shorter wavelen</li> <li>Photonic wirebonds</li> </ul>	gths				<ul> <li>Intro chin onticol interconnect</li> </ul>
			対 Interposer with optical I/O	🕸 Optical interposer wit	h integrated source		<ul> <li>Intra-chip optical interconnect</li> </ul>
		✓ III-V epi on Si ☆ Device scale III-V			-	or templated heteroepitax	win Si-P PDK
			ligned edge coupling in Si-P PDK	Transfer printing of III-		a templated neter depitax	,
	Packaging and Multi-		A Photonics PDK with DFPackaging cont		ackage/chip PDK with thermo-r	mechanical modeling	☆ PDK for co-design of chip and package
	scale Integration	• LTCC			G	.0	
		✓ 2.5D Si-based interposer		Advanced materials a	nd processes for 2.5D Heteroge	neous Integration	
		Flip Chip BGA	🕸 Glass Interposer	<u>के</u> ।	lip chip at fine pitch	-	
		🛱 Fan-Out WLP			☆ Optical int	erconnect in organic subs	strate (PCB)
MATERIALS, DEVICES	Nanofabrication Labs:	🕸 Josephson junction			N-qubit device	<ul> <li>quantum memory</li> </ul>	bry
		<ul> <li>EBL 200 mm Si-P rapid prototyping</li> </ul>	TMDC device	<ul> <li>photonic qubit device</li> </ul>			
	Quantum	☆ post-process relea					
	nanotechnology,	🕸 roll-to-roll process 🖄 2-photon stereolit	• 3D print Si-P ban		arrayed thermal SPL		• multi-beam EB
	processes (linked to	✓ GaN power HEMT		<ul> <li>3D print optical interconduction</li> </ul>	onnect		<ul> <li>CMOS integration</li> </ul>
	microeletronics and	✓ THz antenna ✓ PFIB polish edge w		<ul> <li>graphene FET circuit</li> </ul>			
	photonics)		✓ OG JFET package for liquid sample				
		<ul> <li>Plasmonic structures integrated with PV</li> <li>Plasmonic intercon</li> </ul>	☆ OG JFET on inter	rposer			
		Plasmonic Intercon	nect in SI-Photonics				

	Key technology feature of a planned Product or Service; Development activities are underway and/or supply chain is available.		
	CMC is seeking collaborators, suppliers to deliver capability.		
•	Anticipated technology feature based on roadmap sources.		