Packaging and Multi-scale Integration

2018-2022 Microsystems Technology Roadmap, June 2018

Canada's National Design Network

NDN Technology Space	Year 1	Year 2	Year 3	Year 4	Year 5
	2018	2019	2020	2021	2022
Packaging and multi-scale integration	● Photonic wirebonds				● Intra-chip optical interconnect
	✓ III-V epi on Si	☆ Interposer with optical I/O	☆ Optical interposer with integrated source		
	☆ Device scale III-V bonded to Si	● Wafer scale III-V bonded to Si		● Nanowire or templated heteroepitaxy in Si-P PDK	
	✓ Sub dB passively-aligned edge coupling in Si-P PDK		● Transfer printing of III-V to Si-Photonics		
		☆ Photonics PDK with DFPackaging content	● Package/chip PDK with thermo-mechanical modeling		☆ PDK for co-design of chip and package
	● LTCC				
	✓ 2.5D Si-based interposer		●Advanced materials and processes for 2.5D Heterogeneous Integration		
	● Flip Chip BGA	☆ Glass Interposer	☆ Flip chip at fine pitch		
	☆ Fan-Out WLP			☆ Optical interconnect in organic substrate (PCB)	

The Microsystems Technology Roadmap has 5 segments:
Microelectronics/MEMS/NEMS, Photonics, Embedded Systems, Packaging and Multi-scale Integration, and Nanofabrication Labs.

For more information, contact Robert Mallard (mallard@cmc.ca).

✓	Key technology feature of a planned Product or Service; Development activities are underway and/or supply chain is available.
☆	CMC is seeking collaborators, suppliers to deliver capability.
●	Anticipated technology feature based on roadmap sources.

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