

# Photonics: Silicon-Photonics, III-V, Optics

2018-2022 Microsystems Technology Roadmap, June 2018

Canada's National Design Network



Photonics Technologies		2018	2019	2020	2021	2022
Silicon Semiconductor	SOI	<ul style="list-style-type: none"> <li>★ SOI on 300mm wafers</li> <li>• SOI optimized for long wavelength</li> <li>✓ Si-P rapid prototyping with e-beam</li> <li>• Si<sub>3</sub>N<sub>4</sub> for low loss and/or shorter wavelengths</li> </ul>	<ul style="list-style-type: none"> <li>★ Sub-wavelength structures</li> </ul>	<ul style="list-style-type: none"> <li>• Ge waveguides, Si cladding, 8-10μm</li> <li>★ TSV in Si-P MPW</li> <li>• BIST, ATPG for photonics</li> <li>• Strained Ge for direct gap applications</li> </ul>		<ul style="list-style-type: none"> <li>★ Epi-based III-V gain blocks in SOI PDK</li> </ul>
	Si <sub>3</sub> N <sub>4</sub> /Si/SiO <sub>2</sub>	<ul style="list-style-type: none"> <li>★ Hybrid SOI and Si<sub>3</sub>N<sub>4</sub> platform</li> </ul>			<ul style="list-style-type: none"> <li>• Si-P in "zero change" CMOS</li> </ul>	
Compound Semiconductor		<ul style="list-style-type: none"> <li>★ III-V integration platform</li> </ul>				
Hybrid Integration & Packaging		<ul style="list-style-type: none"> <li>✓ III-V epi on Si</li> </ul>		<ul style="list-style-type: none"> <li>• Transfer printing of III-V to Si-P</li> <li>★ Sub-wavelength structures</li> <li>• Wafer scale III-V bonded to Si</li> <li>★ Optical interposer with integrated source</li> <li>★ Glass interposer</li> </ul>	<ul style="list-style-type: none"> <li>• Nanowire or templated heteroepitaxy in Si-P PDK</li> </ul>	<ul style="list-style-type: none"> <li>• Intra-chip optical interconnect</li> </ul>
	III-V + silicon photonics	<ul style="list-style-type: none"> <li>★ Device scale III-V bonded to Si</li> </ul>				
	Interconnect	<ul style="list-style-type: none"> <li>• Photonic wirebonds</li> <li>✓ Sub dB passively-aligned coupling in Si-P PDK</li> </ul>	<ul style="list-style-type: none"> <li>★ Interposer with optical I/O</li> </ul>		<ul style="list-style-type: none"> <li>★ Optical interconnect in organic substrate (PCB)</li> </ul>	
CAD and Modeling		<ul style="list-style-type: none"> <li>✓ Integrated Si-P CAD tools (schematic/simulation/layout/verification) with IP libraries</li> <li>✓ Schematic-driven Si-Photonics design flow</li> <li>✓ Experimentally verified compact models in Si-P</li> </ul>	<ul style="list-style-type: none"> <li>★ Monolithic photonic/microelectronic PDK</li> <li>• Photonic device package PDK</li> <li>★ Si-P PIC LVS with thermo-mechanical modeling</li> </ul>	<ul style="list-style-type: none"> <li>★ Integrated schematic-driven Si-P and uE PDK</li> <li>✓ Integrated package / chip PDK</li> <li>• Package/chip PDK with thermo-mechanical modeling</li> <li>★ Photonics &amp; Microelectronics co-design flow</li> </ul>		
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The Microsystems Technology Roadmap has 5 segments:

Microelectronics/MEMS/NEMS, Photonics, Embedded Systems, Packaging and Multi-scale Integration, and Nanofabrication Labs.

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✓	Key technology feature of a planned Product or Service; Development activities are underway and/or supply chain is available.
☆	CMC is seeking collaborators, suppliers to deliver capability.
•	Anticipated technology feature based on roadmap sources.