Title: Integrating Machine Learning within FPGA Placement

Speaker: Dr. Shawki Areibi (University of Guelph)

Abstract

In this talk we highlight how Machine Learning (ML) can be integrated effectively within the FPGA CAD flow. Specifically, the placement problem. We first present several Machine Learning and Deep Learning (DL) models for accurately predicting, forecasting and managing congestion within a placement. We then present a novel DL framework based on Convolutional Neural Networks for predicting the routability of a placement. This DL model achieves a routability prediction accuracy of 97% while exhibiting runtimes of only a few milliseconds. The final part of the talk introduces an ML-based framework for recommending the most appropriate placement flow to use for different circuits.

Bio

Shawki Areibi received the B.Sc. degree in Computer Engineering from Tripoli University, Libya in 1984, and the M.A.Sc. and Ph.D. Degrees in Electrical/Computer Engineering from the University of Waterloo, Ontario, Canada in 1991 and 1995 respectively. From 1997 until 1999 he was a faculty member in the Electrical and Computer Engineering department at Ryerson Polytechnic University, Toronto, Canada. Currently, he is a Professor at the University of Guelph in the School of Engineering "Computer Engineering" program. His research interests include VLSI Physical Design Automation, Combinatorial Optimization, Machine Learning, Reconfigurable Computing Systems, Embedded Systems and Parallel Processing. Dr. Areibi is a registered professional engineer in Ontario (P.ENG) and a Senior IEEE member. Dr. Areibi has authored/co-authored over 120 papers in international journals and conferences. He served on the technical program committees for several international conferences on Computer Engineering and Embedded Systems. He also served as a member of the program committee for GECCO, HPC and several other IEEE conferences.