F-517.e

LOWERING BARRIERS FOR NEMS & MEMS TECHNOLOGIES

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Passive Silicon Interposer Platform with TSVs for Multi-Technology Integration

Why interposers?

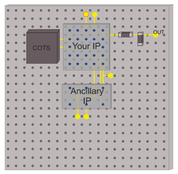
- Digital society demands increasing interconnectedness: power efficiency, compactness, ultra-high-speed computing integration.
- Moore's Law Si scaling is becoming cost prohibitive, relying on advanced packaging to push limits of a tech node.
- Supply trend: more heterogenous integration required for implementation of 5G, and AI.
- BUT, high cost of entry!

	PCB	Interposer
Line width	75 µm (3 mils)	5 µm (0.2 mil)
Line spacing	75 µm	5 µm
Line thickness	30 µm	1 µm
Relative Dielectric Const.	4.3	4
Loss tangent	0.025	0.0015
Spacing between layers	165 µm	1.5 µm
Wiring density	130 lines / cm sq.	600 lines / cm sq.

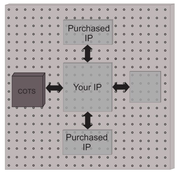
Very small sizes:
- 400µm thickness
- 2 top RDL
- 1 bottom RDL
- 5µm metal width/spacing

- TSV diameter: 100µm
- TSV pitch: 500µm
- $\frac{1}{15}\ Width_{\ PCB\ metal}$
- $\frac{1}{2}\ thick_{bare\ die}$

FLEXIBLE PROTO IP Vendors

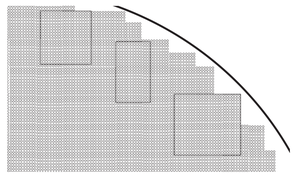


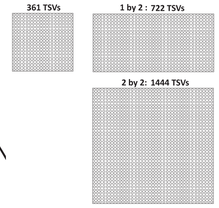
RAPID DEMO SoC Developers



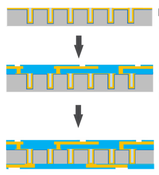
- HW module for evaluation of IP variants
- Close to final product: Speed, Size, Power
- With BGA, interposer unit can be early field unit, then replaced with SoC

Method



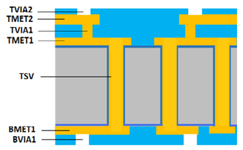


- We start-off with an 8'' wafer
- Pattern (array) TSVs uniformly across whole wafer
- No scribes or free area
- Removes limits to design size
- Standard tiles or custom arrays



Four process modules:
1. TSV Array formation
2. Top-side patterning
3. Bottom-side patterning
4. Component placement

Modular approach:
- Wafer hand-off mirrored
- Finished product
- Intercept manufacturing flow outside of validated network

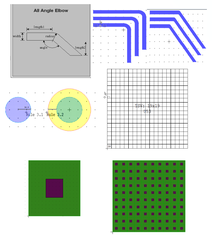


Die interconnect by flip-chip or wire bonding

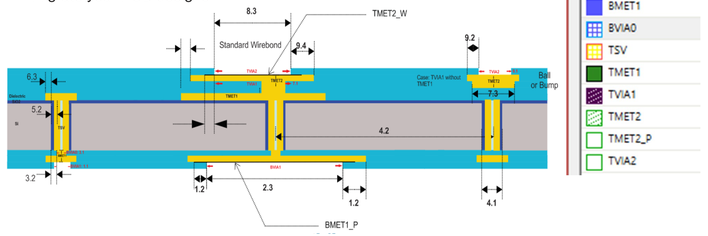
- Ball drop bumping
- Stencil print
- Solder bumping
- Standard BGA: 100µm diameter 1mm pitch
- Underfill

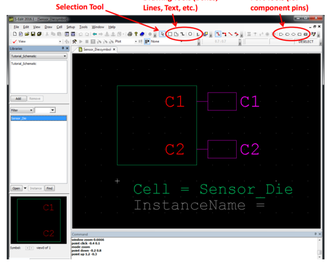
User's Guides, Training Kits, Rules Decks and Design Tutorials

- Tanner Tools currently deployed
  - Curve tools add-on by softMEMS with G-S-G RF trace capability
  - Primitives, Cells for Pads, Contacts, TSV arrays and TSV connections
- Design rules always up to date
- Library of standard components
- Common surface mount and WLCSP footprints

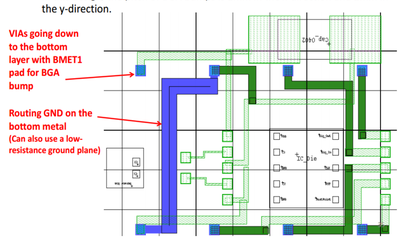


DRC Rules in User's Guide
- Carry-out DRC, LVS before submitting the design
- Migrate your PCB designs



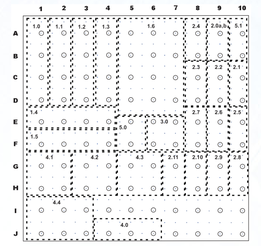


– In this design, the pitch of BGA bumps is 1mm in the x-direction and 2mm in the y-direction.

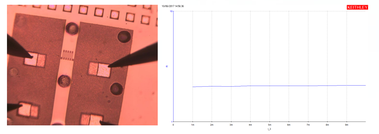


Results

Test chip with Process Control Module (PCM):
- Each supplier fabricates a PCM
- Choosing supplier according to test chip results

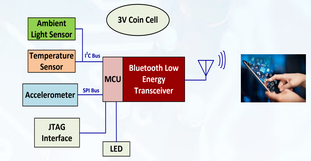


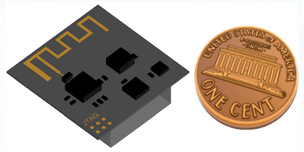
PCM – 4pt resistance



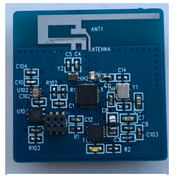
Tests:
- 4-point resistance
- Contact chain
- Max current
- Continuity and Isolation
- S-Params on G-S-G

Reference design 1 – Compact BLE sensor node

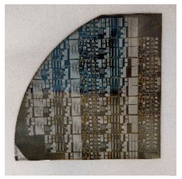




- Light, temp sensors, accelerometer, CC2640 MCU, coin cell
- Antenna incorporated on silicon interposer
- Sharing common blocks of circuitry with users
- Library of schematics, layouts



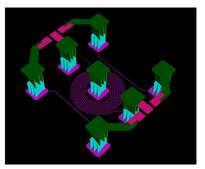
Early PCB prototype



Silicon prototype

Future development

Enhancement to poly Si TSV



RDL variants: Al, Cu, Au

- New era of innovation not just in the chip but the packaging.
- Chip, package, board and system designers manage numerous multiphysics challenges that increase the risk of failure.
- Main issues: power integrity, signal integrity, reliability, electromagnetic cross-talk, thermal-mechanical effects pose significant hurdles for design closure.

About CMC

CAD: PDKs, training

Over 500 CAD tools and modules

Over 5000 individual users annually

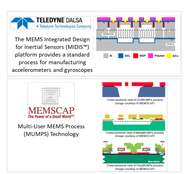
alphacam, Altium, Ansys, ARM, cadence, COMSOL, COVENTOR, CROSSLIGHT, DESIGN WORKSHOP TECHNOLOGIES, IAR SYSTEMS, Intel FPGA, KEYSIGHT TECHNOLOGIES, LUCEDA PHOTONICS, Numerical, Mentor Graphics, nLight, Optiwave, Photon Design, softMEMS, SOLIDWORKS, synopsys, ThermoFisher SCIENTIFIC, XILINX, XpertDesk, Zemax, SEMulator3D

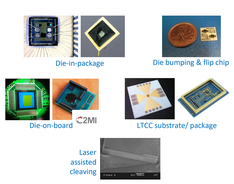
... AND MORE

FAB: MPW services, Packaging & Assembly

amf, Fraunhofer Heinrich Hertz Institut, Lumentum, leti, NRC·CNRC, tsmc, ST, imec, III-V lab, INO, Fraunhofer, TELEDYNE MICRALYNE, TELEDYNE DALSA, Azastra Opto Inc, amf, MEMSCAP, ANT APPLIED NANOTOOLS, CORNERSTONE FOUNDRIES, 3IT, Institut interdisciplinaire d'innovation technologique

MNT Awards (various labs)





LAB: Development systems, equipment rental