Cover letter:

I am recruiting for a project that I am leading

Project Title:

RISC-V Vector Processor for High-throughput Multidimensional Sensor Data Processing & Machine Learning Acceleration at the Edge

This project is a collaboration between Polytechnique Montréal, ETH Zürich, CMC Microsystems, and the OpenHW Group

This is a 3-year project.

We are recruiting : one postdoc, several PhDs and Masters

Required competencies:

Computer architectures, hardware design languages, design flow, FPGA prototyping, ASIC design, support software, accelerators for embedded AI

Interested candidates can send their CV to:

Yvon Savaria

yvon.savaria@polymtl.ca

Project Description:

RISC-V Vector Processor for High-throughput Multidimensional Sensor Data Processing & Machine Learning Acceleration at the Edge
Un processeur vecteur RISC-V pour le traitement de signal et l'intelligence artificielle en bordure du réseau

Project leader: Yvon Savaria , yvon.savaria@polymtl.ca

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A main challenge in advanced computing is increasing the performance of systems while keeping their power envelope within tight bounds, as dictated by the needs of a wide range of applications. This high demand for energy-efficiency, coupled with the limitations of technology scaling – which no longer provides improved performance at constant power densities – is leading designers to explore new microarchitectures. This project will explore this trend by revisiting the vector processing model, which provides a highly efficient way of exploiting data parallelism in scientific and matrix-oriented computations, as well as in high-throughput multi-dimensional digital signal processing and machine learning (ML) algorithms under real-time constraints.

The efficiency of vector processors (VPs) comes from their ability to perform parallel-data computations on very large vectors, thereby amortizing the overhead of fetching and decoding instructions. The starting point for this project will be a VP that follows the specifications of the open-source RISC-V ISA "V" vector extension, and it will take place within a larger research project known as the PULP Platform [1]. Specifically, this project will build on prior works that led to a first-generation RISC-V VP called Ara. The Ara VP is a state-of-the-art parametric in-order high-performance 64-bit vector unit based on version 0.5 of the RISC-V "V" specification, which works in tandem with the Ariane application-class RV64GC scalar processor core. Early analysis of Ara has shown that it achieves up to 41 DP-GFLOPS/W, which is superior to similar vector processors found in the literature. Yet, insights gained with this analysis also highlighted that addressing specific limitations of Ara would significantly improve its energy-efficiency. In addition, Ara must be updated to support the most recent version of the RISC-V "V" extension (from version 0.5 to version 0.9), which is continuously evolving. This project will explore several research areas with the objective of improving the energy-efficiency of Ara.

[1] "PULP Platform - Parallel Ultra Low Power." https://pulp-platform.org/projectinfo.html