Progressing to Prototypes:

Canada's National Design Network®

Designs in Fabrication

April 2017 – March 2018

About CMC Microsystems and Canada's National Design Network®

CMC Microsystems (CMC) works with researchers and industry across Canada's National Design Network (CNDN), providing access to world-class tools, technologies, expertise and industrial capabilities for designing, prototyping and manufacturing innovations in microsystems and nanotechnologies. CMC reduces barriers to technology adoption by creating and sharing platform technologies.

www.cmc.ca

CMC Microsystems' fabrication reports describing Canada's National Design Network designs that have progressed to fabrication are published for distribution at www.cmc.ca

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Table of Contents

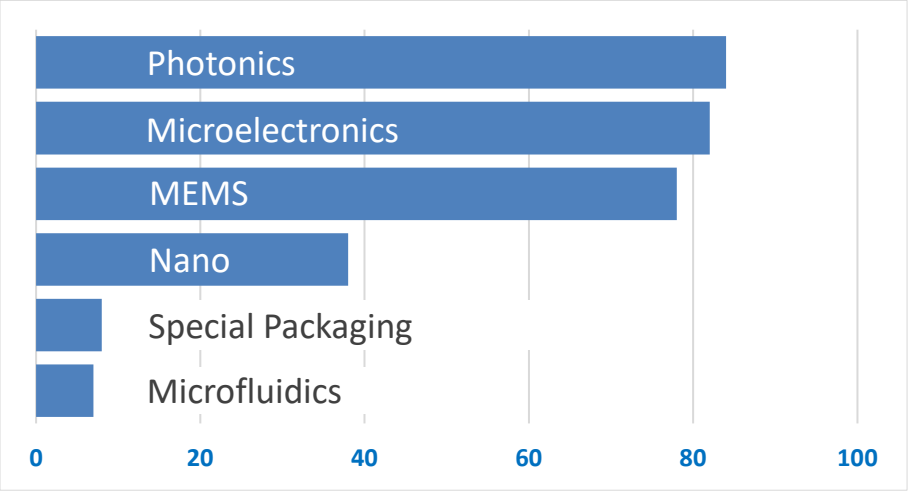
INTRODUCTION

CMC delivers key CAD-FAB-LAB services to increase researchers' and companies' innovation capability in Canada. Support is available for industrial projects and academic R&D.

- **CAD** State-of-the-art environments for successful design – via desktop or CMC Cloud
- **FAB** Services for making working prototypes – MPW and custom fabrication
- **LAB** Equipment device validation to system demonstration – shorten the development cycle

This report describes designs that have progressed to fabrication for prototype purposes within 2017/18. It provides a view into the activities of researchers in Canadian post-secondary institutions – often in the context of applications and solving problems.

Designs in fabrication: 2017/18



Looking for collaborative opportunities?

For further information we encourage you to contact researchers directly or contact us:
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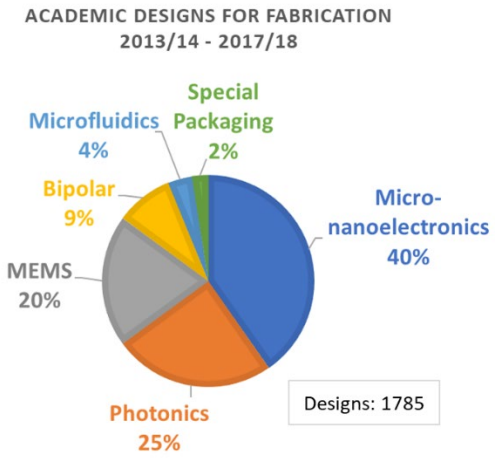
Five-Year Period: 2013/14 through 2017/18

Academic Designs

- **1785** designs progressed to fabrication for prototype purposes through CMC. Academic projects, shown in the figure on the right, included:
  - 719 microelectronics
  - 440 photonics
  - 360 MEMS

Industrial Designs

- Additionally, **68** industrial projects progressed to fabrication. Of these, 43% were fabricated in photonics and 43% were in MEMS technologies.



Photonics & Optoelectronics

By March 2018, over **700** photonics & optoelectronics designs progressed to fabrication for prototype purposes through CMC (2008/9 through 2017/18).

- Silicon photonics fabrication accounted for over **500** designs.
  - More than **60%** of the silicon photonics designs resulted from the Canada-wide advanced training program delivered through UBC/SiEPIC (NSERC-CREATE, 2013-2018), in partnership with CMC Microsystems.
- III-V Fabrication accounted for over **115** of the photonics designs.
- More than **70** projects benefited from CMC's MNT Portal services; and over **60** developmental and commercial projects were prototyped.

FAB Supply Chain

Multi-project wafer (MPW): CMC provides access to some of the best foundries in the world for MPW services, value-added packaging and assembly services, and in-house expertise for first-time-right prototypes.

Custom fabrication: More than **500 prototypes** have been enabled in university-based labs by financial assistance provided by CMC. The lab network includes over 40 labs across Canada, for example:

Simon Fraser University	Université Sherbrooke	Université de Montréal	University of Alberta	University of Toronto	McMaster University	Queen's University

FOR INFORMATION: www.cmc.ca/FAB

MICRO-NANOELECTRONICS

Technology: 65-nanometer CMOS

TSMC 65nm CMOS

4-Channel Phased Array RF Front End for 5G MIMO Beamforming Applications

Applications include: ICT

A reconfigurable 4-channel beamforming transmitter for 5G applications will be submitted. This design incorporates a sub-harmonic injection locked oscillator (SILO) beamforming technique, which can be reconfigured between 28 GHz and 38 GHz 5G application bands using low-loss tunable matching networks. The transmitter consists of a power-efficient reconfigurable power amplifier (PA), a variable gain amplifier (VGA), mixer, and a sub-harmonic injection locked oscillator. In comparison to state-of-the-art RF/LO beamforming system the realized SILO based technique will reduce power and area overhead significantly. Further, it is expected to eliminate design complexity in LO routing and any need of multipliers and buffers.

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TSMC 65nm CMOS

A Highly Tunable VCO for mm-wave Applications

Applications include: Agriculture/Agri-Food, Automotive

A highly tunable VCO for mm-wave applications.

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TSMC 65nm CMOS

A mm-wave Voltage-Controlled Oscillator with High Tuning Range and Low Phase Noise

Applications include: ICT

Voltage-controlled oscillators (VCOs) are indispensable in the operations of fully integrated transceiver architectures. Major design challenges in particular in portable applications include the generation of high-quality quadrature phase outputs with low power consumption and low voltage operation. This also applies to emerging mm-wave applications such as 5G cellular communication, where one would like to achieve a high data rate and thus operate in mm-wave frequency range with a large tuning range while maintaining low-power consumption and low phase noise. Phase noise (which is an indication of the quality and purity of the oscillator signal) trades off with quadrature accuracy and tuning range, at a given power consumption. Motivated by the recent advances in the field of silicon-based mm-wave technology, the focus of this research is on the development of a design methodology for mm-wave VCOs with an emphasis on the low phase noise and low power consumption. Based on the reported state-of-the-art VCOs, transformer-based structures are gaining more popularity and offer added advantages as compared to their traditional cross-coupled and Colpitts designs. Such VCOs offer more design degrees of freedom and thus the design can achieve s better optimal operating point. In this study, a proof-of-concept prototype transformer-based mm-wave VCO structure that is low power, efficient and robust and is low power and low phase noise will be designed, fabricate, and tested.

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TSMC 65nm CMOS

Active Backscattering Tag for Millimeter-wave Localization System
Applications include: ICT

The IC being designed is the core circuit for an active backscattering tag for wireless localization operating at millimeter-wave frequencies. Its prototype built with the commercial off-the-shelf components at a lower frequency is already demonstrated in our lab. It is composed of a low noise amplifier (LNA) and a Gilbert cell modulator. The LNA is cascaded with the modulator through the RF/IF port and a low-frequency (sub-GHz) modulation signal is fed to the LO port. A dielectric resonator antenna out of the chip will be connected to the LNA-modulator chain to close the loop and form an oscillator-antenna. During the operation, the base station (already developed) transmits a chirp interrogation signal. A square wave modulation signal switch on/off the oscillator such that at each starting moment, the phase of the oscillator is synchronized with the interrogation signal. As the frequency of the modulation signal is approaching the chirp bandwidth, the designed tag acts similarly to a passive tag backscattering the interrogation signal but with significant link gain (up to 100dB at 48GHz and 50 meters). Moreover, simultaneous data transmission will be realized by coding the modulation signal (on/off keying or PWM). The phase noise and efficiency are the critical parameters for the design. The out-of-chip antenna acts as a high-quality factor resonator such that the phase noise can be improved by 15dB at 1 MHz offset, compared with traditional oscillator topologies such as Colpitts and common-source cross-coupled differential pair. Moreover, for verification the design and modeling the process, inductors, microstrip resonators, transmission lines, filters and transistors with different size are included in the design. They will help us better understand the dielectric & metal layer property and the transistor performance at our frequency of interest; and they will ensure success of design for future runs of this technology.

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TSMC 65nm CMOS

An Asynchronous Underwater Receiver - Featuring a modular yet supply noise insensitive skew compensation architecture for clock and data synchronization
Applications include: ICT

One of the critical tasks of an underwater receiver is to properly align the reference clock with the incoming data. Increasingly, a lot of post processing circuits including RF/Analog/Digital blocks are being incorporated at the receiver side. Low skew clock and data delivery coupled with stringent limitations on jitter/phase noise are essential to ensure high speed operation in such blocks. Traditional delay locked loop (DLL) based clock/data synchronisation solutions assume matched wire delays and identical delay lines, while achieving supply noise rejection using dedicated voltage regulators. However, increasing circuit densities exacerbate intra-die mismatch, this coupled with worsening thermal gradients for new CMOS technologies makes clock/data delivery to diverse receiver blocks challenging. Moreover, the noise rejection bandwidth of traditional regulator-based techniques is inherently limited by the bandwidth of their active feedback loops. Therefore, the proposed design implements a high-speed underwater receiver featuring a mismatch insensitive clock/data alignment coupled with an innovative regulator less supply rejection technique. The receiver features an adaptive delay locked loop (DLL) architecture which can eliminate clock skew resulting from control code dependent mismatch in delay lines or wire delays, regardless of process, voltage or temperature variations. Additionally, supply noise rejection is achieved by appropriately biasing a compensation circuit whose supply sensitivity is opposite to that of the delay cells constituting a DLL delay line, thus bypassing the bandwidth limitations of an active feedback loop. Moreover, the proposed design is modulator i.e. clock delivery to a new circuit node can be achieved by simple coupling to the nearest synchronised node without needing explicit source matching. The proposed DLL works at 1GHz and achieves a lock time of under 50 cycles while consuming 2.5mW of power at 1V.

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GF 0.13µm CMOS

An Integrated Dual-Band Radio-Frequency Energy Harvesting Interface for Biomedical Wearable Devices
Applications include: Health/Biomedical, Natural Resource/Energy

In this design, a low-voltage and fully integrated RF energy harvesting system, in 130 nm CMOS technology is presented. The system uses ISM bands 915 MHz and 1900 MHz as inputs with sensitivity of -32 dBm. A 10 stages cross-coupled rectifier with dynamic threshold voltage compensated is designed to convert a very low input RF power (-21 dBm) to the 1 V DC voltage at 1 Mohm resistor load. Then, a power management unit (PMU) is designed as interface between transducer and load to match voltage and current of the RF front end and load, supply voltage regulation and minimize the power consumption.

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TSMC 65nm CMOS

Blocker Adaptive Segmented Receiver
Applications include: ICT

It is a segmented LTE band receiver (1-3GHz), which can adaptively change its Linearity and Noise performances based on the blocker activity. This helps in power saving, because having both high linearity and low noise usually comes at a power expense.

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TSMC 65nm CMOS

Design and Implementation of Low-Complexity Mixed-Signal Decoder
Applications include: ICT

We plan to implement a mixed-signal decoder circuit that replaces 17-input adders traditionally implemented with digital circuitry, with much simpler analog circuits. Unlike digital addition and storage in conventional min-sum or modified differential decoding (MDD), the proposed architecture uses current-mode addition and continuous charge storage on a capacitor. The changes reduce power dissipation but come at the cost of analog impairments. Therefore, our claim for improvements in the target metrics must be validated experimentally through IC fabrication. To prove improvement in the throughput of the decoder, consecutive decoding cycles must be run quickly one after another. This requires enough on-chip memory to store digital input bits and rapidly feed them into the decoder. The layout placement of the main decoder section has been fully automated using cadence SKILL code. Furthermore, the decoder length in the horizontal direction has been effectively compressed four times based on empirical characteristics of the sparse decoder description matrix. The distance between logic gates and wiring connections has been carefully chosen to meet minimum DRC requirements.

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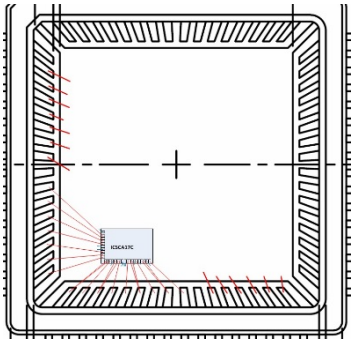
TSMC 65nm CMOS

Design of High-Speed, Configurable, Area- and Power-Efficient CMOS Optical Receiver
Applications include: ICT



This work aims to design a low-noise, high-speed area- and power-efficient optical receiver for chip-to-chip interconnects. This project includes three PhD students and consists of two main parts. The first part is a re-spin of a chip fabricated in September 2016. We have done extensive testing this year on the previous chip and have learned from previous designs and have thought of new methods to improve the receiver. The second part is a novel design for the receiver front-end to be low-noise avoiding explosion in power consumption and chip area. This project is focusing on a re-configurable optical receiver for source-synchronous links. It will involve the design of a new phase skewing method for clocking circuitry, implemented in a newly proposed architecture designed to improve silicon photonic (SiP) links. The methods aim at improving the yield of SiP chips using reconfiguration of CMOS chips. For the data circuitry, a novel multi-level active feedback technique is adopted to extend the bandwidth without using the conventional passive inductors. This technique allows to design dense, low-noise receiver circuits.

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TSMC 65nm CMOS

Design of High-Speed, Configurable, Area- and Power-Efficient CMOS Optical Receiver
Applications include: ICT

This work aims to design a low-noise, high-speed area- and power-efficient optical receiver for chip-to-chip interconnects. This project includes three PhD students and consists of two main parts. (The first part is a re-spin of a chip fabricated in September 2016.) We have done extensive testing this year on the previous chip and have learned from previous designs and have thought of new methods to improve the receiver. The second part is a novel design for the receiver front-end to be low noise avoiding explosion in power consumption and chip area. This project is focusing on a re-configurable optical receiver for source-synchronous links. It will involve the design of a new phase skewing method for clocking circuitry, implemented in a newly proposed architecture designed to improve silicon photonic (SiP) links. The methods aim at improving the yield of SiP chips using reconfiguration of CMOS chips. For the data circuitry, a novel multi-level active feedback technique is adopted to extend the bandwidth without using the conventional passive inductors. This technique allows to design dense, low-noise receiver circuits.

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TSMC 65nm CMOS

FD-PC Phase Shifter
Applications include: ICT

The IC is a special type of phase shifter/frequency divider designed for a novel phased array antenna at Ku-band.

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TSMC 65nm CMOS

Four Channel 20Gb/s Optical Receiver

Applications include: ICT

This design is focused on the electronics a hybrid (silicon photonics with CMOS) four channel 20Gb/s optical receiver. The optical input can be delayed through a silicon photonics delay-line chip. By using four optical delay elements, four optical signals with different delays are resulted. These optical signals are then passed to four separate optical receivers. By carrying out some signal processing on the output of different receivers, it can be shown that the required data-rate of each receiver is 1/4 of the total data rate of the input optical signal. Hence, the total optical link can work at a much higher data rate than what the CMOS technology node would traditionally support. This project aims at a low-rate demonstration to establish a proof-of-concept. Here, the input signal power is divided between the delayed signals, resulting in trade-offs between sensitivity, data rate and power consumption.

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TSMC 65nm CMOS

Fully Integrated Hybrid Buck/boost Converters

Applications include: ICT

This project aims to design and compare the performance of two integrated inductors both implemented in the TSMC 65-nm technology. The first inductor is a conventional square inductor. The second inductor is a chamfered inductor (a shape between a square and a regular octagon that optimizes the inductance time-constant ratio). The two inductors are integrated in two identical hybrid buck/boost converters to prove the improvement of the performance of the proposed shape. Each converter circuit has its own control circuitry and oscillator. Both the buck and boost converters use the same pair of switches which saves area overhead without sacrificing efficiency. The goal of this project is to validate the feasibility and reliability of the proposed design and to demonstrate that using the proposed shape of inductor can improve the conversion efficiency without sacrificing the inductor's area. The project also targets maximizing the power density and minimizing the output voltage ripple.

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TSMC 65nm CMOS

Hierarchical On-Chip Millimeter-Wave Wireless Micro-Networks for Multi-Core Systems
Applications include: ICT

A W-band receiver for multi-band wireless network-on-chip will be designed. The receiver consists of a wideband high-gain LNA, and tuned-rectifier-based envelope detector, and a low-power inductorless baseband amplifier. The LNA uses active Gm boosting to achieve high gain with low noise figure and power consumption. The rectifier is based on a passive topology designed for wide bandwidth and good conversion gain. This rectifier departs from standard envelope detector designs for OOK demodulation to conserve power and improve the efficiency of the receiver. The baseband amplifier relies on a combined feedback and feedforward technique to improve bandwidth with minimal power and area overhead. A W-band transmitter will also be submitted based on a direct modulation VCO and high efficiency wideband drive amplifier. The direct modulation VCO uses a pulse generation technique paired with envelope shaping feedback to dramatically reduce start-up time and improve direct modulation capabilities. The direct-modulation VCO achieves 16 Gb/s modulation data rate, allowing excellent power efficiency per transmitted bit. We will also investigate energy savings in compressed sensing by using cognitive time domain ADC architectures with embedded matrix multiply and accumulate front-end for efficient in-node signal processing. Such sensors employed in biosensing and neurosensing can help reduce massive computations at higher level nodes by transmitting only when edge sensors recognize new data is meaningful. Such cognitive transmission improves energy efficiency by cutting down on massive raw data processing.

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TSMC 65nm CMOS

High-speed Area- and Power-efficient PAM-4 Receiver for Short-reach Optical Links
Applications include: ICT

This work consists of two parts. The first part is a re-spin of a 2015 chip which implements a PAM-4 optical receiver. The second part is our ongoing research in designing high-performance optical receivers and VCSEL drivers. In 2015, we designed a low-power optical PAM-4 receiver, which consists of a novel analog front-end and quadrature rate decision circuits. We also designed a novel tuning scheme of three threshold levels of the decision circuits to optimize the bit error rate performance of the receiver. The second part of this project is to design a limited-bandwidth front-end followed by a novel equalizer stage to achieve better sensitivity and power-efficiency with avoiding the limitation of the prior work. The two-tap feedforward equalizer presented in [1] amplifies the high-frequency noise relative to the signal power, resulting in a degradation of the signal-to-noise ratio. The FIR decision feedback equalizer-based receiver in [2] can achieve good sensitivity due to the high-gain, limited-bandwidth front-end, high power-efficiency due to the absence of the power-hungry main amplifier, and high area-efficiency due to the lack of passive inductors. However, it suffers from a timing constraint problem that limits the speed to 4 Gb/s. The continuous time linear equalizer-based receiver in [3] succeeded to achieve excellent sensitivity at 25 Gb/s but it uses passive inductors and consumes a huge amount of power. Our proposed design will explore continuous-time inductorless equalization.
[1] M. H. Nazari and A. Emami-Neyestanak, "A 24-Gb/s Double-Sampling Receiver for Ultra-Low-Power Optical Communication," IEEE Journal of Solid-State Circuits, vol. 48, no. 2, 2013.
[2] A. V. Rylyakov et al., "A new ultra-high sensitivity, low-power optical receiver based on a decision-feedback equalizer," in Optical Fiber Communication (OFC), Los Angeles, CA, pp. 1-3, 2011.
[3] D. Li et al., "A Low-Noise Design Technique for High-Speed CMOS Optical Receivers.

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TSMC 65nm CMOS

Highly Linear-efficient Power Amplifier for 5G Applications

Applications include: ICT

The focus of this research is to implement a low-power high-performance mm-wave power amplifier that is suitable for next generation wireless communication systems and beyond. According to Cisco Systems Inc., a global leader in communications and Internet solutions and services, mobile data traffic will grow 10-fold globally between 2014 and 2019, reaching 24.3 Exabyte (one billion gigabytes) per month worldwide in 2019. Consequently, since current generation of mobile communication standards (4G) will no longer be able to accommodate the needs of customers in the near future, the next generation standard (5G) is being developed. In fact, 5G is expected to provide Internet connections 40 times faster and with at least four times more coverage worldwide than the current 4G Long Term Evolution (LTE) wireless communications standard. One of the critical and power-hungry building blocks of such transceivers is their power amplifier and the focus of this research is on the design of a low-power and highly linear PA (operating in 30 GHz band) that is suitable for portable devices.

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TSMC 65nm CMOS

Idea to Innovation (I2I) Hybrid Optoelectronics Receiver

Applications include: ICT

A high-speed, energy efficient optoelectronics receiver is being developed. This receiver employs a technique that allows parallel processing of high-speed optical data and a capacitive front-end. With this technique and the parallel processing of optical data, superior energy efficiency can be achieved. The target speed of this receiver is 40Gb/s and the energy efficiency is below 1pj/bit. This receiver is distinguished from the first two generation though the inclusion of more gain stages which allows the receiver to operate at a higher data-rate (10Gb/s of the first generation and 25Gb/s of the second generation). We expect a better sensitivity as well. It is also distinguished in that it includes electronic delay elements which improve receiver immunity to process variations in the photonic integrated circuit. By having part of the delay done electronically and the other part done optically, receiver sensitivity and energy efficiency improve. It also allows the speed to go beyond the 25Gb/s limit seen in the second generation. Many components of the receiver have been revised an optimized for better operation relative to the first two generations. This chip is the third-generation receiver of an on-going NSERC-funded Idea to Innovation (I2I) project.

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TSMC 65nm CMOS

Integrating Circuits and Antennas

Applications include: ICT

The chip being fabricated integrates different prototypes of active integrated antennas operating at millimeter-wave/sub-THz frequencies. It is a continuation of a PhD research work that demonstrates the next generation of highly integrated, low loss and reconfigurable millimeter-wave/sub-THz front-end systems. The active antenna array (the chip) merges both amplification and antenna properties into a single device, i.e., simultaneously amplifies and radiates the millimeter-wave/sub-THz signal, resulting in higher integration and lower losses. The DC bias variation helps in achieving the reconfigurable features of beam steering and frequency tuning. So far, the concept has successfully been analyzed and demonstrated at 5-GHz, and we are certain that it performs even better at sub-THz and millimeter-wave frequencies (our intended design bands) for upcoming and future applications of millimeter-wave/sub-THz technologies in wireless communications such as 5G technologies and systems which are being discussed and developed worldwide.

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TSMC 65nm CMOS

Low-Power 60-GHz Receiver for Phased-Array Systems

Applications include: ICT

Although beamforming modems have become popular in high-speed data transmission using Standard IEEE 802.11ad, it is still challenging to utilize them in portable devices such as smart phones due to their relatively high-power consumption. To overcome this issue, we propose a low-power structure for a 60-GHz receiver. The proposed technique is based on reducing radio frequency (RF) signal's path loss. As a result, less power will be consumed to compensate for this loss. More specifically, a combination of RF- and LO-path phase shifting without using phase rotators or phase interpolators is applied to reduce power consumption. The receiver chain consists of a low-noise amplifier (LNA), switched-type phase shifter (STPS), mixer, phase selector and a variable gain amplifier.

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TSMC 65nm CMOS

Millimeter-wave Doppler Radar System for Noncontact Vital Signs Detection
Applications include: ICT

The IC being designed is the core circuit for a millimeter-wave Doppler radar system for noncontact vital signs detection. Its prototype built with the commercial off-the-shelf components at a lower frequency is already demonstrated in our lab. According to the theory, the use of an electromagnetic wave with higher frequency (and smaller wavelength) may have better phase-modulation sensitivity. This increased sensitivity may allow for better breathing and heartbeat signals to be extracted from the millimeter-wave vital signs detection system than from the lower frequency systems. In addition, at the higher millimeter-wave frequency range, a smaller chip size could be developed for the CMOS detector. The chip being designed is composed of a transmitter and a receiver. The transmitter consists of a voltage-controlled oscillator (VCO), an image-rejection up-converter and a power amplifier (PA); the receiver consists of a low noise amplifier (LNA), a down-conversion mixer and a baseband amplifier. A pair of patch antennas out of the chip will be connected to the PA output port and the LNA input port, respectively, to form a millimeter-wave radar transceiver system. The transmitter transmits a millimeter-wave single-tone continuous-wave (CW) signal, which is reflected off a target and then demodulated in the receiver. According to the Doppler theory, a target with a time-varying position but a net zero velocity will reflect the signal with its phase modulated proportionally to the time-varying target position. CW radar with the chest-wall as the target will receive a signal similar to the transmitted signal but with its phase modulated by the time-varying chest-wall position. Demodulating the phase will then give a signal proportional to the chest-wall position that contains information about movement due to heartbeat and respiration.

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TSMC 65nm CMOS

Non-coherent Two-way IR-UWB Ranging Device
Applications include: Agriculture/Agri-Food, Health/Biomedical, ICT

This chip contains the full system of an impulse-radio ultra-wideband (IR-UWB) ranging device for wireless short-distance ranging applications, operating in the 3.1 GHz to 6 GHz spectrum. The proposed two-way ranging device functions via a non-coherent strategy. The goal of this device is to get a below 10 cm accuracy in a multi-path environment.

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TSMC 65nm CMOS

PAM-4 VCSEL Driver and Receiver for Short-reach Optical Links/Variable Bandwidth front-end with Variable Jitter CDR for Optical Link Receiver

Applications include: ICT

This project consists a PAM-4 VCSEL driver, a PAM-4 receiver, and a novel receiver front-end. In the receiver part, a limited-bandwidth front-end followed by an equalizer stage will be used to achieve better sensitivity and power-efficiency compared to the regular full-bandwidth design. The well-known feedforward equalizer amplifies the high-frequency noise relative to the signal power, resulting in a degradation of the signal-to-noise ratio. On the other hand, a decision feedback equalizer-based receiver can achieve better sensitivity due to the use of a clean previously resolved bit(s) in resolving the current bit. However, it suffers from a timing constraint and error propagation problems. Our proposed design will explore continuous time inductorless equalization breaking the speed limitation. This VCSEL driver design is targeting at optical transmission in PAM-4 pattern. Flexible multi-tap equalization is applied to perfect the distorted pulsed, thus, to mitigate ISI caused by nonlinearities during the transmission process. For both MSB and LSB paths, each desired tap impacts on both 2 rails and employs adjustable tap width, occupying certain ratio of signal interval; also, each tap height is only related to that tap's strength, not being the sum of some taps' heights. As been said, the taps effects on upper and lower rails can be asymmetric, and this highly adjustable asymmetric equalization indicates the flexibility points. The third part of this tape-out consist of two main circuit blocks. The first will be a variable bandwidth front-end and the second will be a variable jitter CDR. The variable bandwidth front-end targets the reconfigurability of the bandwidth to be such that during the change in the bandwidth, the data remain aligned with the recovered clock to have minimum bit error rate. This CDR will incorporate a power and phase noise reconfigurable VCO to achieve lower power consumption at lower data-rate.

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TSMC 65nm CMOS

Phase Conjugating Phase Shifter (PCPS)

Applications include: ICT

The IC is a special type of phase shifter designed for a novel phased array antenna at Ku-band.

University of Waterloo

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TSMC 65nm CMOS

Radiation Effects Analyzation on PLL Sub-circuit and Rad-hardened PLL Design

Applications include: ICT

PLLs have many applications in integrated circuits and systems ranging from agile frequency synthesis, clock recovery circuits, and local oscillator (LO) frequency generators. The main role of the PLL is to generate an output signal at a specific frequency. The basic PLL system consists of the phase detector, loop filter, voltage-controlled oscillator, and the fractional divider. For electronics and communication systems used in space, the PLL circuits are exposed to radiation which can have a catastrophic effect on the system. Due to the transients caused by heavy ions, sensitive components of the PLL such as the VCO will operate incorrectly. Single event transients (SETs) will impact the PLL circuits causing phase and frequency shift, which can result in loss of PLL frequency lock. In this project, different sensitive sub-circuits of the PLL will be fabricated separately to investigate the radiation sensitivity of each sub circuits. Charge pump is one of the most sensitive components of the PLL to single events. Two rad-hardened charge pumps will be proposed in this project to analysis the anti-radiation effectiveness. If the charge pump functional block is hardened to a sufficient level, the VCO becomes the dominant SE upset source. Not only does the VCO result in the most detrimental SEUs in the PLL, but the VCO has the greatest cross-section, indicating that the majority of the single event transients (SETs) generated in the PLL will be due to strikes in the VCO. RO (ring oscillator) based PLL has a wider range of operation, simple structure and smaller circuit area. While the LC-tank oscillator usually requires more silicon but has outstanding phase noise and jitter performance with narrow range of operation. The LC tank and RO oscillators will be fabricated separately for the radiation effects analysis. A fully integrated radiation hardened PLL will also be implemented in 65nm process for radiation analysis.

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TSMC 65nm CMOS

Receiver for SKA 41-antenna Array Demonstrator

Applications include: Aerospace

The Micro/Nano Technologies (MiNT) Laboratory at the University of Calgary is developing ultra-low noise receivers for use in high-sensitivity antenna arrays, such as those needed for the next generation radio telescope, known as the Square Kilometre Array (SKA). The development of such a receiver is nearing the stage of passing our designs to interested industrial partners for manufacturing. However, a few design challenges still need investigation. The main challenge is to demonstrate its operation as part of a phased array receiver. The first stage of this verification study is to place the receivers in a 41-element array. The key performance metric to be investigated is the receiver performance under the influence of array noise coupling. This is very difficult to simulate accurately, as the array dimensions are large and full 3D EM simulation is prohibitively computationally intensive.

University of Calgary
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TSMC 65nm CMOS

Wide Tuning Range VCO for 100Gb/s High-speed Links

Applications include: ICT

The aim of this project is to design a VCO that spans a tuning range of 20.8GHz to 31.2GHz over PVT corners, with a low phase noise and power consumption for 100Gb/s multi-rate high-speed links.

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Technology: 130-nanometer CMOS

GF 0.13µm CMOS

0.1-12GHz Frequency Synthesizer for Avionic SDR Applications

Applications include: ICT (avionic SDR application)

The proposed design is a frequency synthesizer architecture for avionic software defined radio (SDR) applications. The synthesizer provides a carrier frequency range from 100 MHz to 12 GHz covering the avionic communication applications and existing wireless standards. The switched-capacitor (SC) voltage-controlled oscillator (VCO) that the output frequencies are derived from is implemented covers a wide tuning range from 8 GHz to 12 GHz. The VCO ensures high phase noise performance with low power consumption. The transient phase locked loop (PLL) response shows a reduced settling time whereas the PLL loop bandwidth is of about 600 kHz. Furthermore, the synthesizer exhibits a phase noise, simulated at 12 GHz, of -104 dBc/Hz at a 1 MHz frequency offset with an overall power consumption of 14.88 mW.

École de technologie supérieure
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GF 0.13µm CMOS

10-Bit SAR ADC with Improved DAC Switching Scheme

Applications include: Environment, Health/Biomedical

This 10-bit successive approximation analog to digital converter reduces the number of required unit capacitors from 1024 required for a binary weighted ADC to 25. The DAC sub-component uses the charge sharing method to produce the required analog values to compare to the signal. It is controlled by a finite state machine whose logic was determined using a novel algorithm implemented in Matlab. The reduction in the number of unit capacitors results in a smaller chip area and improved power consumption.

Carleton University
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GF 0.13µm CMOS

A 256x256 CMOS Image Sensor for Pixel-Wise Focal-Plane Computational Imaging

Applications include: Automotive, Defence (Safety, Security), Entertainment, Health/Biomedical

In the last decade, CMOS image sensors have become the dominant video acquisition technology. Due to their moderate cost, CMOS imagers are an attractive choice for multi-sensor applications such as wireless sensor networks. In such applications the high amount of optical computations are impossible on the image sensor plane. Image computation tasks such as compressive sensing and pattern recognition require bulk optical relay modulators and high-volume off-sensor image processing. The primary objective of this design project is to build up a programmable CMOS image sensor with on-chip imaging computation features. Through novel pixel structure and sensor architecture, both optical computations and image processing are implemented directly on the image sensor chip to significantly reduce the camera packaging size and the burden of image processor.

University of British Columbia
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GF 0.13µm CMOS

A Fully Integrated Multiple-Output Step-Down Switched-Capacitor Voltage Regulator for System-on-Chips

Applications include: Health/Biomedical, ICT

This design forms a novel fully integrated multiple-output switched-capacitor voltage regulator (MOSCVR) for use in system-on-chips (SoCs). SoCs contain various functional circuit blocks which require different supply voltages for their optimal performance. Moreover, utilizing multiple supply voltages can effectively reduce power consumption. Hence, the use of the proposed MOSCVR can meet the requirement of multiple supply voltages in SoCs to enhance performance and energy savings. Additionally, the proposed topology that will be implemented in the MOSCVR reduces power loss thus enhancing power efficiency compared with conventional approaches of using multiple independent SCVRs.

University of British Columbia
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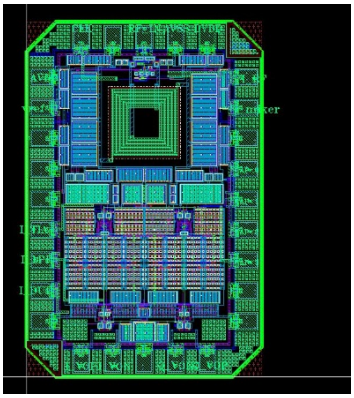
GF 0.13µm CMOS

A Low-Power Receiver Front-End for Zigbee Sub-GHz Applications

Applications include: Automotive, Defence (Safety, Security), Entertainment, Environment, Health/Biomedical



This project aims to implement a sub-GHz RF receiver front-end for Zigbee standard. The front-end consists of a low noise amplifier, mixer, transimpedance amplifier and low pass filter. The goal of this research is to investigate novel approaches to simultaneously achieve low power, low noise and high linearity performance in the receiver. The highlight of this design is the use of class AB operation in multiple design blocks which results in high blocker tolerance.

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GF 0.13µm CMOS

A New Charge Pump with Enhanced Current Drivability

Applications include: Health/Biomedical

Recently, battery-powered portable devices, such as cell phones, tablet computers and portable measurement instruments etc. have been experiencing rapid increase. For these applications, voltages higher than the battery supply voltage tend to be needed. Switched-capacitor DC-DC step up converters, also known as charge pumps, can obtain different DC output voltages by transferring charge among capacitor networks using clock phases. Compared with the traditional inductor-based buck converters, charge pumps benefit from the significantly higher energy density of capacitors over inductors. Their inductor-less feature makes them especially suitable for chip-level power conversions. The designed charge pump is composed of two branches and each branch has 10 stages. Two out-of-phase clock signals are used to boost +1.2V input voltage to +8V while delivering several milliampere load current. This charge pump can obtain an improved power efficiency when driving large load current by reducing the undesired charge transfer. Voltage pumping gain is also increased by keeping threshold voltage drop and body effect eliminated.

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GF 0.13µm CMOS

Application of Slow Wave Inductors in Injection Locking Oscillators

Applications include: (wireless communication)

This work is an extension to the previous design where novel inductors based on Slow Wave technique were designed. The miniaturization achieved in the size of the inductors, a vital electronic component in most RF circuits, necessitates testing their performance in a practical situation. One of the useful applications, which is widely used in different transceivers is the Injection Locking Oscillator. The good performance of this circuit from different points of views gives the motivation to apply the previously designed inductors in it. One of the drawbacks of this circuit is the relatively large sized inductors used consuming a large area on the chip. Consequently, this design is aiming at following the research trend in achieving chip-size reduction which will directly reflects its benefits on the fabrication cost.

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GF 0.13µm CMOS

Energy Harvesting Uncertain Double-sampling Receiver

Applications include: Health/Biomedical, ICT

The main objective of this design is to implement energy harvesting uncertain double-sampling receiver for smart stents, i.e., stents with embedded sensors. Due to the physical size limitations and the nature of the applications (stents being implanted in arteries) efficient energy harvesting and RF receiver are of paramount importance. Based on preliminary analysis and calculations, the system should be able to operate from 0.5V supply and consume sub 30-uW. The proposed techniques and topologies can also be applied to other low power applications such as biomedical implants, wireless sensor networks and Internet-of-Things applications.

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GF 0.13µm CMOS

Fully Implantable Neural Recorder and Stimulator
Applications include: Health/Biomedical

This project is focused on the design, simulation and experimental characterization of an ultra-low power wireless and battery-less implantable microsystem to be used for neural recording and stimulation. The system will have 128 small area, low-noise, high resolution recording channels to interface with the brain. A signal processing and machine learning engine within the system will support the detection of various neurological events and adapt to a range of environmental factors. By combining the co-processor with a neural stimulation block, it is possible to provide therapy for severe neurological disorders such as Alzheimer's disease, Parkinson's disease and epilepsy. Machine learning offers many new prospects including patient specific adaptation, overcoming motion artifacts and responding to biological changes over time. We intend to expand the architecture found in [1] to include the use of phase-based features to improve detection performance. The recorded data can be transmitted to a computer using on-chip wireless transmitters or fed to the signal processing unit to trigger event-based electrical stimulation to the brain. The system will be powered using an on-chip receiver coil which removes the need for a battery. The same on-chip coil will be used to receive commands to control the chip.

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GF 0.13µm CMOS

High-bandwidth Low-current CMOS Integrated Sensors for Nanopore DNA Sequencing
Applications include: Health/Biomedical, Pharmaceutical (and applied physics research)

The proposed design consists of a transimpedance amplifier (TIA) to convert small-amplitude (10-100 pA) input current pulses produced by a nanopore or a cellular ion channel to large output voltages for eventual digitization and readout. The TIA is designed to have a low thermal noise floor (less than 10 fA/rtHz) and a wide bandwidth (above 2 MHz). The TIA architecture consists of an integrator stage followed by a differentiator stage to acquire the signal in continuous mode. Since the dc component of the input current could lead to integrator saturation, a new switching scheme is proposed to avoid this issue while allowing the input signal to be observed in a continuous manner. In addition, a differential system architecture will be implemented to increase SNR. Capacitance compensation through bootstrapping is also used to reduce the apparent input capacitance of the TIA which will further enhance the overall bandwidth of the recording channel.

University of Waterloo
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GF 0.13µm CMOS

High-resolution CMOS Neural Interface for Synchronized Optogenetics and Electrophysiology (I)
Applications include: Health/Biomedical

In this project funded by NSERC, CIHR and the Weston Brain Foundation, we will develop a CMOS brain implant on a chip that will condition, detect and compress on-line the neural activity. This system on a chip will detect the presence of action potentials, or spikes i.e. electrical activity of the neurons, and further compress those detected waveforms. The compression will be performed using a wavelet transform based algorithm to achieve high compression ratio (>= 500), allowing to transmit the data from more channels than previous systems while using fewer resource and lower power. Used in conjunction with the previous successful design, the system will provide both high-resolution multimodal electrophysiological recordings and synchronized optogenetic photo-stimulation capability (stimulation will be synchronized with the detected neuronal activity) for studying brain microcircuits of transgenic mice. The present design provides an innovative multichannel spike detection algorithm and a multichannel wavelet compression algorithm, both implemented in this SOC. The prototype includes five main building blocks: (1) a multichannel digital spike detector module, (2) a RAM memory module, (3) a multichannel Symmlet-2 wavelet transform module, (4) a multichannel compression module, and (5) a serial peripheral interface (SPI) module. This proposed design represents the second step towards the realization of a complex mixed-signal brain implant on a chip including a microcontroller and all the necessary analog and digital modules to perform closed-loop optogenetics within a single chip. This SOC will be used to study the brain of freely behaving mice through an application paradigm related to the discovery of therapeutics against neurodegenerative diseases of aging with our partners at the Québec Mental Health Institute Research Center (CRIUSMQ) in Québec City.

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GF 0.13µm CMOS

High-resolution CMOS Neural Interface for Synchronized Optogenetics and Electrophysiology (II)
Applications include: Health/Biomedical

In this project funded by NSERC, CIHR and the Weston Brain Foundation, we will develop a CMOS brain implant on a chip that will condition, detect, compress and sort on-line the neural activity. This system on a chip will detect the presence of action potentials, or spikes i.e. electrical activity of the neurons, and further compress and sort those detected waveform. The spike sorting (or clustering) will be performed using a new algorithm that will take advantage of the wavelet-based compression algorithm and the spike detector designed previously. Compared with existing solutions, the spike sorting algorithm will be computed on-chip and will require no manual threshold settings i.e. it will be all automated. With this feature, the IC will be able to determine from which neurons each detected spike was issued. Used in conjunction with the previous successful design, and the other design (above), the system will provide both high-resolution multimodal electrophysiological recordings and synchronized optogenetic photo-stimulation capability (stimulation will be synchronized with the detected and sorted neuronal activity) for studying brain microcircuits of transgenic mice. The present design provides an innovative multichannel spike sorting algorithm. The prototype includes three main building blocks: (1) a multichannel digital spike sorting module, (2) a RAM memory module, (3) a serial peripheral interface (SPI) module. This proposed design represents the third step towards the realization of a complex mixed-signal brain implant on a chip including a microcontroller and all the necessary analog and digital modules to perform closed-loop optogenetics within a single chip. This SOC will be used to study the brain of freely behaving mice through an application paradigm related to the discovery of therapeutics against neurodegenerative diseases of aging with our partners at the Québec Mental Health Institute Research Center (CRIUSMQ) in Québec City.

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GF 0.13µm CMOS

Hybrid Digital LDO and Buck Converter Envelope Modulator

Applications include: ICT

This design forms a novel Digital LDO (DLDO) based hybrid envelope modulator for use in envelope tracking systems. The use of a DLDO makes the design inherently resilient to chip-to-chip variation and allows lower voltage operation as compared with traditional modulator implementations. Additionally, the controller implemented in the proposed DLDO provides faster transient response and thus wider bandwidth than is achievable in conventional analog designs, thus allowing envelope tracking to remain viable for efficiency enhancement in the next generation power amplifiers (PAs) for cellular systems.

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GF 0.13µm CMOS

Implantable On-Chip Bio-sensing & Impedance Imager

Applications include: Agriculture/Agri-Food, Health/Biomedical, Pharmaceutical

Biosensing and Electrical Impedance Tomography are less explored schemes in medical imaging which utilizes low frequency electric field spectrum to map 3D compositions of body tissues. This technique has been proven effective for intensive care lung conditions such as the Acute Lung Injury (ALI), alternatively detectable only by CT scans. While the other medical imaging systems such as the CT scans and MRIs offer higher resolution, they cannot be used in the realm of integrated circuit (IC) based microsystems to enable the creation of implantable medical devices that can alarm early signs of the diseases. EIT on the other hand, is based purely on electrical network analysis which can be implemented independently and with great precision in standard CMOS. We are proposing a fully wireless implantable EIT imager for monitoring tissue permittivity for early detection of cancer cell regrowth after surgery. The 4mm bare die will be implanted or injected in the surgical site after removal of tumor. In addition, the proposed chip includes fully integrated transmitter that enables injectable platform for drug level and glucose monitoring that can be utilized in personalized therapy.

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GF 0.13µm CMOS

Inductor Size Reduction using Slow Wave Technique

Applications include: ICT (wireless communication)

Chip size reduction is one of the most important research trends. Consequently, the constraints imposed on the passive on-chip components became more severe because they consume most of the chip size. On chip inductors are one of the essential lumped components that are used in most of the electronic circuits. Its performance is a critical issue for the designed circuits to work well. Quality factor, inductance per unit length, parasitic capacitance and size are important parameters to be considered in its design. On the other hand, transmission lines designed using the Slow Wave concept have been dramatic with the best results showing sizes reduced to about 30% of the original size. To exploit this Slow Wave effect, this work is intended to test the feasibility of miniaturizing the size of on-chip inductors.

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GF 0.13µm CMOS

Integrated Biochemical Sensor Platform
Applications include: Pharmaceutical

The project integrates an array of biological as well as chemical sensors to be able to perform a complete biological assay in less than 20 minutes. This chip is a complete system chip, with optimizations related to interfacing with and measuring the chemical environment, including multiple measurement channels.

University of Toronto
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GF 0.13µm CMOS

Integrated Power Management Circuit for MEMS Energy Harvesters
Applications include: Environment, ICT

MEMS based energy harvesters have seen a growing interest in recent years as they can provide a clean source of energy in vibrational environments (e.g. cars, airplanes, car tires, air ducts, bridges etc.). To extract the power from the harvester, specialised power conditioning circuits are required. In this design, a circuit is proposed to provide high efficiency, very low input voltage operation, good load regulation and sufficiently high DC output voltage requirements for a piezoelectric MEMS vibration energy harvester. A combined cross coupled rectifier and a switched capacitor DC-DC converter is designed to provide a stable DC power supply (1.2 V) to bias wireless sensor systems.

Université du Québec à Montréal (UQAM)
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GF 0.13µm CMOS

Low Drop Out Regulator with Integrated Bandgap Reference

Applications include: Health/Biomedical

The proposed LDO with integrated bandgap reference can operate for VDD as low as 0.6 V and generate 0.5 V reference voltage for load ranges from 0 to 5 mA. The power consumption is less than 10 uW. The design of the LDO is based on current mode feedback technique and the overall loop gain is enhanced by the combination of TIA and voltage amplifier in the loop. The output voltage is temperature independent since it is the combination of PTAT and CTAT voltage components. The PTAT and CTAT current generators are merged into the LDO to provide the ability of temperature compensation by injecting the PTAT/CTAT current into the resistor at the output node.

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GF 0.13µm CMOS

Millimeter Wave Configurable Transmitter for Phased Array Systems

Applications include: Automotive

A configurable transmitter front end for Millimeter wave wideband application with a power detector that is integrated to an off-chip directional coupler.

University of Waterloo
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GF 0.13µm CMOS

Quad-Level Carrier Width Modulation Demodulator for Micro-Implants

Applications include: Health/Biomedical

This project aims to implement a new demodulator based on Quad-Level Carrier Width Modulation (QCWM). This fully integrated QCWM demodulator allows high data-rate transmission at ultra-low power consumption. It includes a Pulse Width to Saw-tooth Peak (PW to SP) Converter. The envelope of the received signal is detected by an envelope detector structure exploiting a PW to SP converter followed by a voltage comparator and a low-voltage reference. Also, the envelope of the modulated signal, a square waveform, is retrieved for synchronization purposes. Afterwards, the retrieved output signal is compared with three different voltage references. Then, the three comparators are fed to a 3 to 2 sequential logic decoder in order to assess the exact received bit-words.

Polytechnique Montréal
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GF 0.13µm CMOS

Ultra-Low-voltage (<0.6V) Amplifiers with Extremely Wideband
Applications include: ICT

The design of RFICs in the ultra-low voltage (<0.6 V) regime poses challenges for low noise and low distortion operation. While the noise figure of a low-voltage amplifier can be brought to very low levels over a narrow band, broadband low-noise performance is more difficult to achieve. In this design, we seek to demonstrate a low-noise amplifier having an extremely wide fractional bandwidth of 20:1 (50 MHz to 1 GHz) operating from a 0.6 V supply. A second amplifier will be included on the same die that operates from 0.2 GHz - 2 GHz that will exhibit an IIP3 of greater than +12 dBm.

Queen's University
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GF 0.13µm CMOS

Wireless-powered Receiver for Biomedical Implants
Applications include: Health/Biomedical

The design includes a wireless receiver module and a wireless power front-end module. The chip is intended to operate in 900MHz band and will be powered by modulated carrier. The harvested wireless power will be rectified by the rectifier block and the data will be demodulated by the receiver, which includes a passive mixer, amplifier, clock and data recovery circuit and digital control blocks. In addition, an ultra-low-power transmitter (TX) designed for biomedical implants will be also implemented.

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Technology: 180-nanometer CMOS

TSMC 0.18µm CMOS

A High Dynamic Range CMOS Biophotometry Sensor with an Extended Counting ADC

Applications include: Health/Biomedical

In this design, we will develop a high-dynamic range optoelectronic biophotometry sensor with extended counting ADC all integrated inside a CMOS system-on-a-chip (SoC). This SoC will be the core of an implantable and high-precision optical neural interface microsystem. In fact, fluorescence biophotometry measurements require wide dynamic range (DR) and high sensitivity measurement tools. This design provides these key characteristics to collect Ca2+ ionic transfers resulting from brain activity within freely moving animal photometry scheme. In addition, it will provide optogenetic photo-stimulation as well for enabling optogenetically-synchronized fiber photometry. For that purpose, a micro-LED driver will activate an LED to illuminate neurons, expressed by genetically encoded calcium indicators, through a brain-inserted multimodal fiber. The fiber will be coupled to the micro-LED and with the high-dynamic range bio-photometry sensor to collect the evoked neural activity. The developed device will be evaluated in-vitro and in-vivo at the CERVO center to validate and to measure its functionality and performance.

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TSMC 0.18µm CMOS

Bio-impedance Sensor Array with Lock-in Amplifiers

Applications include: Health/Biomedical, Pharmaceutical

Bio-impedance measurement is a fully electronic technique to determine the physical and chemical properties of live cells under varying environmental conditions. Although optical measurement platforms are widely used for cell imaging, these systems normally require labeling cells with fluorescent molecules, which can alter cellular properties. However, impedance measurement obviates the need for fluorescent tags but with the disadvantage of reduced measurement SNR. We will implement a CMOS sensor array to extract the impedance of individual cells directly on the chip surface. The chip will contain a 100x100 array of 50-µm^2 noble-metal surface microelectrodes, formed through CMOS post processing, which will be in physical contact with live cells. Each electrode will be multiplexed to a column-parallel 1 kHz-10 MHz lock-in amplifier with on-chip low-pass filters and ramp-based ADC. We aim to achieve a relative error in measured impedance magnitude and phase of less than 10% over the measurement bandwidth. We will also take advantage of the relatively slow response time of cells to changing environmental conditions to construct a compact, high-performance readout architecture for the lock-in amplifiers.

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TSMC 0.18µm CMOS

Dual-Band Microwave Components for Wireless Applications.

Applications include: (wireless communication)

In this design, a Dual-Band folded mixer with fully integrated multilayer LTCC (low temperature co-fired ceramics) passives and a Dual-Band folded mixer with passives inside the chip are presented. The 180nm CMOS technology is used for implementation. The mixer has been designed for the ISM bands operating at (900) MHz and (2.4) GHz.

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TSMC 0.18µm CMOS

High Density Neural Interface

Applications include: Health/Biomedical

This transceiver will later be integrated in a CMOS system-on-a-chip (SOC) that will be used inside a fully implantable, multimodal and high-resolution brain implant. This design is essential. It will provide proper clock and control signals and provides regulated supply voltages.

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TSMC 0.18µm CMOS

Implantable High-Precision Wireless Optical Neural Interface Biophotometry Sensor

Applications include: Health/Biomedical

In this design, we will develop a CMOS system-on-a-chip (SoC) optoelectronic biosensor based on charge accumulation and a current-based technique which will be the core of an implantable and high-precision optical neural interface microsystem. Such a novel microsystem will be key to collect Ca2+ ionic transfers resulting from brain activity within freely moving animal photometry scheme. In addition to providing wireless data to the base station through a custom-designed radio frequency (RF) transmitter, this SoC will provide high-sensitivity fluorescence optical recording along with optogenetic photo-stimulation for enabling optogenetically synchronized fiber photometry. For that purpose, the SoC includes a micro-LED driver to illuminate neurons, expressed by genetically encoded calcium indicators, through a brain-inserted multimodal fiber, which is coupled to the micro-LED and to the high-precision bio-photometry sensor, to collect the evoked neural activity. An ultra-low-power, spectrum-efficient, and power scalable 2.4-GHz radio frequency RF transmitter will be designed to transmit neural data to a base station. The developed device will be evaluated in-vitro and in-vivo at the CERVO center to validate and to measure its functionality and performance.

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TSMC 0.18µm CMOS

Integrated Biochemical Sensor Platform

Applications include: Pharmaceutical

The project integrates an array of biological as well as chemical sensors to be able to perform a complete biological assay in less than 20 minutes. This chip is a test chip for evaluating the chemistry of the CMOS process related to the chemical sensing.

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TSMC 0.18µm CMOS

Passive Switched-Capacitor Filter with Impedance Transformation and Passive Amplification
Applications include: ICT

A configurable order lowpass filter having passive amplification and impedance transformation with complex conjugate poles is implemented using passive switched capacitor circuits. The filter order is configurable in between second and third, and have 4, 3, 2, 1, 1/2, 1/3, and 1/4 selectable gain options, which results in impedance transfer from input to output. This configurable filter design is suitable for filtering and amplification of down-converted signals of re-configurable wireless RF receivers.

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TSMC 0.18µm CMOS

Quadrature-VCO with Tail Injection Superharmonic Coupling
Applications include: ICT

The proposed circuit uses a new method for generation of the quadrature sinusoidal signals through current injection by tail transistors, referred to as tail injection super-harmonic coupling QVCO (TISC-QVCO). Two in-phase (I) and quadrature (Q) oscillators are coupled at their second harmonic by two pairs of tail transistors. This coupling method creates 180 degrees phase difference in the second harmonic, thus, in the fundamental oscillation frequency, 90 degrees phase difference is achieved. The circuit also offers tail current shaping for phase noise reduction. For proper operation, i.e., quadrature coupling and tail current shaping, high-swing output signals as well as triode region operation of tail transistors are necessary.

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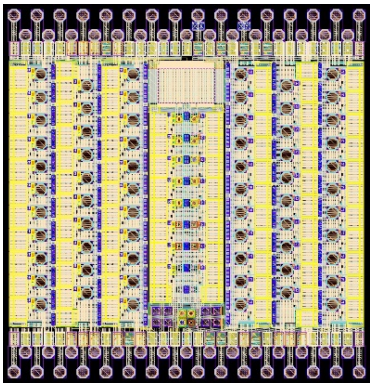
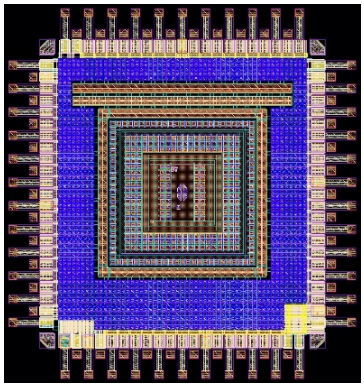
TSMC 0.18µm CMOS

Single Photon Avalanche Diode Array Readout Circuit (I, II, and III)

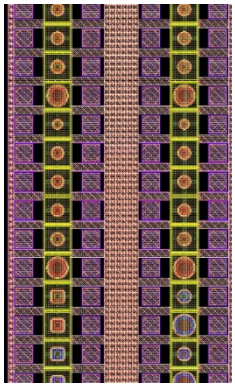
Applications include: Health/Biomedical (high energy physics)



(I)



(II)



(III)

The Groupe de Recherche en Appareillage Médical de Sherbrooke (GRAMS) is working on Single Photon Avalanche Diode (SPAD) based photodetectors integrated in 3D over CMOS electronics. The 3D architecture allows having heterogenous technologies (e.g. optoelectronics coupled to high-end CMOS electronic readout) and hence maximize the detector's performance. The market of these photodetectors is found in many applications such as medical imaging (positron emission tomography), 3D cameras and low light/low background physics experiments. The proposed design is crucial for developing the optoelectronic layer (the SPAD layer) since it will be used as the SPAD readout electronics for their characterization. Of course, the GRAMS already has other SPAD readout circuits (for example in 65 nm), but these circuits can only be used in a 3D configuration, meaning a fully developed SPAD layer and a 3D bonding process. Furthermore, they have limited high voltage capabilities (3.3V max). The proposed readout circuit, built in the TSMC 180 nm BCD CMOS technology, will allow the SPAD to be tested either in a 2D or in a 3D configuration with a higher voltage range for a complete SPAD characterization. This circuit is mandatory for the SPAD development line. It will provide a SPAD test bench with different types of quenching circuits containing low-jitter comparators. Therefore, SPAD properties will be studied with these circuits such as Dark Count Rates (DCR), Single Photon Timing Resolution (SPTR), Photon Detection Efficiency (PDE), crosstalk, afterpulse and so forth.

Université de Sherbrooke

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Technology: 350-nanometer CMOS

AMS 0.35µm CMOS (Base/OPTO)

A CMOS Image Sensor for Pixel-Wise Focal-Plane Coded Exposure

Applications include: Aerospace, Automotive, Entertainment, Health/Biomedical

Focal plane coded exposure refers to an active exposure technique where coding is applied to the light illumination on the image sensor (the sensor domain). To acquire a coded image, a sequence of binary mask patterns is applied in lockstep to control sensor's exposure. Previous research in computational imaging has shown that coded exposure is a very effective method in actively probing light transport and can therefore provide many potentially promising imaging applications such as separating direct and indirect light paths based on the number of reflections, eliminating scattered light, improving the accuracy and/or power efficiency of structured light and other 3D imaging systems. In this work, we design pixels with the embedded SRAM memories which are responsible for applying the exposure codes. The exposure binary code (mask) can therefore be loaded for exposure, resulting in a pipelined coding operation which does not interfere with the pixel exposure time. The mask loading is done serially via a vertical metal line (one line per-column), making both the image sensor and the pixel array scalable towards high pixel resolutions.

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TSMC 0.35µm CMOS

CMOS-compatible Polymer-based Memory Structures

Applications include: ICT (memory)

The objective of this project is to fabricate a memory device on a CMOS chip. This memory is fully functional, capable of addressing to different bits, doing the read and write operations, refreshing the cells, etc. The memory will have arrays of metals and each bit of it will be formed by growing the polymer junctions on top of the arrays of metals.

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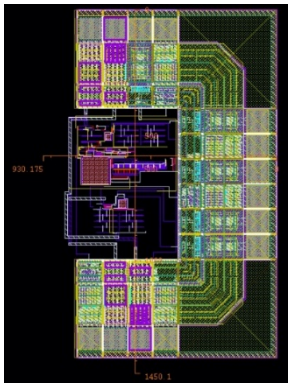
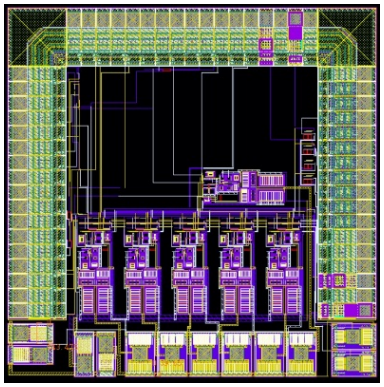
AMS 0.35µm CMOS

CMOS Integrated 2D CMUT Array Towards 3D Ultrasound Imaging (I, II, and III)

Applications include: Health/Biomedical



(I and II)



(III)

We aim to develop CMOS analog front-end (AFE) receiver integrated with capacitive micromachined ultrasound transducers (CMUTs) for high frequency 3D ultrasound imaging. Different from preamplifiers in previous work that are mainly targeted for 2D imaging with bandwidth of only 10 MHz, the current design has targeted bandwidth of 80MHz. Considering device specifications from CMUTs, the Trans-Impedance Amplifier (TIA) is designed to amplify received signals from 10MHz to 150MHz with center frequency at 80MHz. In one typical ultrasound imaging channel, the AFE receiver consists of a TX/RX protection switch, and a readout preamplifier (i.e. TIA in our system). Following the preamplifier, the receiving path also includes Time-Gain Compensation (TGC), Low-Pass Filter (LPF) and Analog-to-Digital Convertor (ADC), and signal processing to obtain the final ultrasound image. The integrated circuit consists of an array of 16x16 channels to amplify and process the signal received by each CMUT element.

Polytechnique Montréal

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TSMC 0.35µm CMOS

CMOS Olfactory Sensors Platform

Applications include: ICT (platform technology applicable to many different market sectors)

This project is the ninth in a series (ICDMB001-8) for an integrated chemical sensor array by using a standard Complementary Metal Oxide Semiconductor (CMOS) silicon fabrication process. This project has been used for training of 3 students in the past and a Ph.D. student is continuing. A patent disclosure has been filed for this technology and we are in discussions with [international companies] for possible commercialisation of this technology. With the past runs we have a tested platform of circuits that includes standard row/column decoder and multiplexer circuits as well as specially designed operation amplifiers, current mirrors, trans-impedance amplifier and A/D converters used to process output from our floating gate sensors. In the present run we plan to optimise the existing circuits to improve the performance of integrated system developed with previous runs.

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TSMC 0.35µm CMOS

Enhancing Performance of MEMS Micromirrors and SPM

Applications include: ICT (optoelectronics)

The CMOS MEMS AFM has demonstrated the ability to image at the nanometer scale. We have developed various tip sharpening processes using previous designs such that very fine features can be resolved during the imaging process. However, the vertical resolution has been limited by the performance of the piezoresistors. The SNR is low due to the low sensitivity of the polysilicon piezoresistors. In these devices, new structural methods will be used to adjust the neutral stress plane such that the sensitivity of the piezoresistors can be enhanced. Through simulation, the enhancements of sensitivity reach almost an order of magnitude. In addition, new mechanical flexures will be used to make the XY stage operate in a much more linear fashion, increase stiffness without sacrificing scan range, resulting in a robust MEMS scanner. Finally, new diffractive optical elements (DOE) will be designed, functioning as an optical MEMS device. Previously, the DOE can focus a beam of light at a fixed focal length. A new design is created such that the focal length can be adjusted based on applied voltage.

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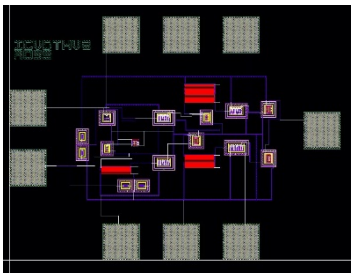
AMS 0.35µm CMOS

High Voltage ASIC Driver

Applications include: ICT (astronomical)



The proposed design implements an increasingly popular technique in analog circuit design, which combines the desirable properties of a continuous-time (analog) circuit with those of a switching mode (digital) design. Our application involves the development of a dedicated ASIC voltage driver chip that is motivated by the increasing demand for an adaptive optics (AO) system scalable to the largest class of optical/NIR telescopes. In this design, the digital input signal (e.g. from a wave front sensor (WFS)) will undergo digital-signal processing (DSP) in which a pulse-width modulation (PWM) or delta-sigma modulation technique will be used to encode the desired signal into pulses. Once this occurs, the signal will be suitable to input into a high-voltage (HV) switching mode driver, a commonly used driving option in MEMS applications. A prototype switching mode driver that minimizes the use of problematic HV transistors and can provide a +/-15 V bipolar signal to drive an array of electrostatic actuators has been designed. The design implements a series of inverter stages with increasing size standard buffer cells to condition the drive signals before applying them to the HV transistors at the output. This increases the load driving capability of the circuit and allows us to use a minimal number of HV transistors. The HV transistors required at the output stage are subject to a highly stable drive pulse between 15 V and 11.7 V that is achieved using a HV transistor and a voltage divider consisting of two large resistors at the input. The overall result is that for a pulsed input signal between 0 V and 3.3 V, a bipolar +/-15 V output signal is produced.

Dalhousie University

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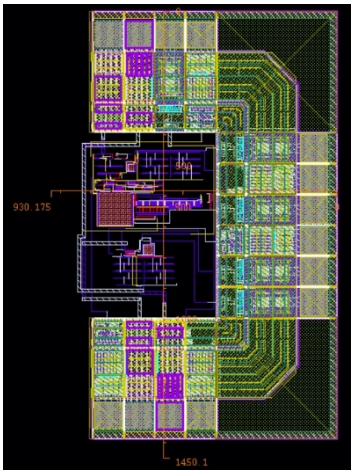
AMS 0.35µm CMOS

High-Voltage Front-End Interface for Single Photon Detectors (SPADs)

Applications include: Health/Biomedical



We aim to design and implement a fully integrated high-voltage (HV) front-end for Single Photon Avalanche Diodes (SPAD). SPADs are widely used for time-domain (TD) functional near-infrared spectroscopy (fNIRS). Generally, SPADs require a high reverse bias voltage for being able to detect low intensity of incoming photons, whereas the other peripheral circuits (comparators, Driver, ADCs etc.) work at relatively low voltages. The proposed front-end generates a voltage varying from 15V to 30V, which can be easily integrated into SPAD probes so that they can work with a single supply voltage of 3V. The proposed design includes a programmable HV dc–dc converter (HVDC), a drive amplifier, and a tuneable pulse generator.

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AMS 0.35µm CMOS

Integrated Ultrasonic Imaging System

Applications include: Health/Biomedical

A battery driven highly-integrated ultrasonic imaging system will be implemented for medical applications. Previously, an array of piezoelectric micro-machined ultrasonic transducers has been fabricated using PiezoMUMPs technology (Design name: IMPQMROB). This time, the control circuit using the high voltage CMOS technology CMOSP35/HV (AMS) will be fabricated. Ultrasonic transducers must be activated by relatively high voltage signals. Hence, control circuit for ultrasound transducers need high-voltage supplies and are therefore difficult to integrate and cannot be powered by a battery. The novelty of the system resides in the fact that it needs solely a battery of 3.6V. To do so, the control low voltage pulses will be level shifted to attack a high-voltage output stage. Then, a charge pump will be used to generate the high-voltage DC needed by the output stage. Finally, a transimpedance amplifier (TIA) is used to amplify the echo signal and a Tx/Rx switch is used order to protect the TIA from the high signals when emitting.

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AMS 0.35µm CMOS (Base/OPTO)

Mantissa-Exponent Image Sensor

Applications include: ICT (neuron monitoring)

Image sensor with embedded floating-point capture and tone mapping algorithm.

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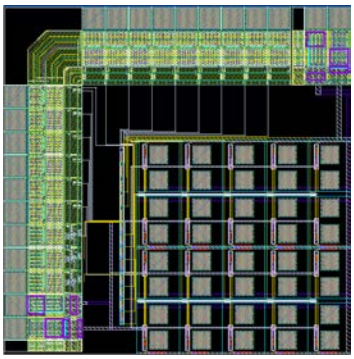
AMS 0.35µm CMOS (Base/OPTO)

Microsystems for Vision Enhancement through Optogenetic Retinal Prosthesis

Applications include: Health/Biomedical



In this project, we aim to develop an active control module (Chip A) to drive a micro-led array. A serial communication block is designed to receive data with the required speed and send them to the driver array at the desired time intervals. The driver array consists of 4x4 driver pixels each which drive the corresponding micro-led from another chip. The micro-led array will be further flip-chip mounted on the fabricated chip. A shift-register block is also designed to perform the addressing of the driver array. L-shape of the ESD protection and bond pad rings allow us to assemble four chips in a single package to increase the size of array.

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AMS 0.35µm CMOS

Multimodal CMOS Biosensor Array

Applications include: Health/Biomedical

This design includes an array of 10x10 capacitive sensors, 10x10 pH sensors for biological sensing purposes. Our team has already demonstrated the advantage of capacitive sensors for bacteria growth monitoring and proliferation of cancer cells" E. Ghafar-Zadeh et al. Bacteria Growth Monitoring Through a Differential CMOS Capacitive Sensor, IEEE Transactions on Biomedical Circuits and Systems (Volume: 4, Issue: 4, Aug. 2010)", " G. Nabovati, E. Ghafar_Zadeh et al. Towards High Throughput Cell Growth Screening: A New CMOS 8 × 8 Biosensor Array for Life Science Applications, EEE Transactions on Biomedical Circuits and Systems (Volume: 11, Issue: 2, April 2017)". In this design, we will study the practical issues affects the performance and sensitivity and demonstrate the full functionality of system for cell culture monitoring using two different types of sensors.

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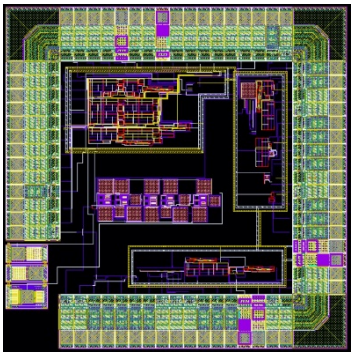
Professor: Ebrahim Ghafar-Zadeh Email: egz@cse.yorku.ca

AMS 0.35µm CMOS

System-on-Chip Time-domain Functional Near-infrared Spectroscopy based on Silicon Photomultipliers

Applications include: Health/Biomedical



We aim to develop a compact probe for time-domain (TD) functional near-infrared spectroscopy (fNIRS) based on a fast silicon photomultiplier (SiPM). High harvesting efficiency can be achieved by exploiting the whole SiPM numerical aperture and can also be put directly in contact with the sample, thus significantly reducing complexity by avoiding the need of optical fibers for light collection. We will integrate an avalanche signal amplification stage optimizing the signal immunity to electromagnetic interferences. The probe will also be equipped with Vertical Cavity Surface Emitting Laser (VCSEL) with a repetition rate over 80MHz and picosecond pulse width. The proposed system can be most effective for TD fNIRS spectroscopy in terms of temporal resolution, responsivity, linearity, and capability to detect deep absorption changes.

Polytechnique Montréal

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PHOTONICS & OPTOELECTRONICS

Technology: III-V Epitaxy

Azastra

AlInAs on InP
Applications include: ICT

Heterostructures based on AlInAs epilayers with low non-intentional doping (NID) levels are required on semi-insulating (SI) InP substrates for optoelectronic and photodetector applications.

Université de Sherbrooke
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Azastra

High-performance Tunnel Junction Structures for Concentrated Photovoltaic Applications (Part II)
Applications include: Natural Resources / Energy

The tunnel junction (TJs) heterostructures need to be grown and fabricated into ~3mm x 3mm photovoltaic (PV) cells, as per previous design of experiment. We request that the structures be manufactured using a commercial concentrated PV (CPV) fab process. The structures have been designed to have a high quantum efficiency in the near infrared range where several high-power diode lasers are available to systematically test the TJ performance (808nm, 830nm, 850nm). The LCSM lab within the 3IT in Sherbrooke is equipped for lab testing with laser diodes between 1W and 20W optical outputs and different wavelengths. The laser diodes setup is capable of exceeding the current densities of today's state-of-the-art CPV solar cells. Some of our industrial collaborators are already working at sun concentrations with high peak intensities of several 1000 suns to lower the cost of CPV systems. The two additional structure variants requested will allow to further quantify the TJ improvements achievable by optimizing the doping of the related layers in a first phase of this project. After the lab testing using the laser diodes, in a second phase, the manufactured cells will be tested outdoor under high sun concentration on the 3IT on-sun setups and/or in collaboration with some of our partners. Requesting 6" (150mm p-type GaAs ~ standard 625microns thickness). 1wafer of 2 runs with different TJ designs hereby provided to extend the parameter range studied in the initial phase.

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Landmark

Hybrid QWI InP Laser Diodes on SOI for 3D PIC Application

Applications include: ICT

One of key elements in 3D photonic integrated circuit (PIC) is integrated silicon laser source. The general objective of the research project is to design and fabricate 3D PIC device which hybrid Distributed Bragg Reflector (DBR) tunable laser diode on silicon on insulator (SOI) material and using taper butt coupler for optical communication between InP laser diode and photonic circuits on SOI substrate. In this project, an InGaAsP compressive strain quantum well (QW) microstructure emitting at 1.30 μm will be used. UV laser induced quantum well intermixing (QWI) will be used first to selective area modify the bandgap in the active region. Also, to reduce the absorption loss, UV laser QWI will enlarge the bandgap in the passive region, e.g. grating region in DBR laser diodes. A butt coupler will be designed to transmit optical signal from InP laser diode to photonic circuits in SOI. Taper coupler structures, UV laser QWI will modify the refractive index in gradient step along transmission direction, which can enhance the coupling efficiency in a more compact structure. We will investigate to enhance the coupler taper efficiency by optimizing UV laser irradiation conditions. Another challenging step is bonding III-V tunable laser diode on SOI substrates. One biggest issue of recent bonding technique like molecular bonding and adhesive bonding is heat dissipation. So, we will investigate Femtosecond (Fs) laser direct bonding of InP on SOI. Fs laser beam will directly focus in the interface between InP and SOI and induce melting. With external pressure, the InP and SOI will bond to each other. We will investigate the bonding strength by optimizing laser conditions.

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Technology: Silicon Photonics – Active & Passive Silicon on Insulator (SOI)

IME SOI

8-channel Fast Wavelength Selector for Applications in Wavelength Division Multiplexing (WDM) Communication Systems

Applications include: ICT

Our submission is a silicon photonic integrated circuit (Si-PIC) for an 8-channel fast wavelength selector for applications in Wavelength Division Multiplexing (WDM) communication systems. The wavelength selector is designed to dynamically select any channel wavelength from an input light source consisting of a comb of discrete wavelengths in the C-band (1530 – 1570 nm). The technical challenges addressed in the design are to achieve wide tunability across the full C-band, to achieve fast average switching speed (< 10 us) from one wavelength to another, and to demonstrate scalability and large-scale integration of Si-PICs. The Si-PIC consists of two arrays of 8 microring resonator (MR) filters, each capable of tuning to any wavelength in the C-band. At the input port, a 1x2 beam splitter is used to divide an input comb of WDM wavelengths into two streams, which are fed to the two arrays of filters. Each MR filter is a Vernier cascade of 2 MR stages; each stage is thermo-optically tuned using microheaters. The outputs of a pair of MR filters, one from each filter array, are combined through a 2x1 fast pin MZI switch, which is used to switch the signal from either filter to the output. Each pin MZI switch employs a differential driving scheme on the two arms of the MZI to reduce the drive voltage and increase the switching speed. Target switching time of the MZI switches is < 10 ns. At any instant in time, only one filter in each pair will be selected (on) and the other will be off. The wavelength selection time can be reduced by pre-tuning a filter to the desired wavelength during its "off" time and then switched to the output when required. The submitted circuit is based on a previous design but with improved pin MZI switch and MR filter designs, much greater complexity and larger scale of integration. In particular, the circuit is scaled up to 8 channels, each filter consists of a 4th-order Vernier design that can provide tunability over the C-band.

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IME SOI

100 Gb/s Optical Front-end for Co-packaging with Low-bandwidth TIA

Applications include: ICT

Project 1: The 100 Gb/s optical front-end leverages the higher bandwidth features of the optical domain and is co-designed for on-chip or off-chip optoelectronics and lower bandwidth CMOS electronics. The optical chip is to be used towards data communication applications with line rates of 100 Gb/s towards the standardization effort by the industry of 400G and 1T Ethernet. This SiP front-end is co-designed with the CMOS IC design chip developed for tape-out in Fall 2017. We observed unexpected behavior of photodiodes (PD) on both 1502PH and 1601PH runs. We aim to resubmit those designs. We will also investigate the behavior of some passive components such as resistors and capacitors and also low-pass RC filters on the SiP dies. These can be further used in manipulating CMOS IC bandwidth. The influence of the bypass capacitor on its adjacent PD bandwidth also needs to be further explored.
Project 2: Ongoing interest toward high-speed communication has resulted in significant interest toward complex modulated data signals. Consequently, coherent detection techniques have been widely used in today's optical telecommunication systems for optical phase characterization. The drawback of these techniques is that a reference laser source along with a power-hungry digital signal processing (DSP) unit need to be implemented at the receiver side. This in turn results in increased complexity and more importantly extensive power consumption at receiver. In our proposed method we implement a Mach-Zehnder interferometer (MZI) as a photonic differentiator. The two signals at the output ports of MZI are then fed into a balanced photodetector (PD). The signal at the output of the balanced PD is proportional to instantaneous frequency (time derivative of phase). On the other hand, having a delayed copy of the signal under test (SUT) and utilizing simple accumulative integration on the acquired instantaneous frequency, the phase profile of SUT can be simply characterized.

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IME SOI

A 0-40 GHz Silicon Photonic Integrated RF Receiver with Low Phase Noise Characteristics

Applications include: Aerospace (Non-Defence), Defence (Safety, Security)

The aim of this research is to develop a silicon-photonics-based 0-40 GHz tunable RF receiver with high performance, chip-scale form factor, remoting capability, and enhanced environmental stability for targeting the requirements of next-generation RF spectrum scanning and analysis systems. In fact, future lightweight and high demanding platforms require the highest level of performance and chip-scale integration at the same time. Unfortunately, microwave technology is revealing unable to achieve the target performance with the desired level of compactness due to its intrinsic bandwidth constraints. In a similar way, current microwave-photonic solutions, in order to solve the problem of the system phase noise introduced by the laser sources, rely on RF or optical components that prevent a chip-scale integration. Instead, the high-performance-receiver design proposed in this project stems from a digital phase-noise cancellation technique able to remove the phase noise introduced by laser sources exploited in the scheme and, at the same time, avoids all the RF/optical components that prevent miniaturization, enabling a full chip scale integration through silicon photonic platform.

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IME SOI

Amplified Silicon Photonics

Applications include: ICT

In order to instigate a major advance in optical link budget management we propose research on efficient, low-cost and scalable integration of optical amplification moving beyond "loss-less" links via amplified Silicon Photonics. Our aim is to produce external optical amplification of ~15-20dB within SiP systems at wavelengths in the O, C and L bands; plus, around 1960nm, a wavelength which centers on a prospective communication window and is currently under intense research. Rare-Earth amplifiers can bring their well-established benefits to silicon- based systems, namely, their high-bit-rate amplification, broad gain, low cost, and low noise figures. The key challenges of such amplifiers are building them in a silicon-compatible manner and developing compact devices with sufficient gain lengths for the required amplification. Recent work addressed the former challenge through the development of a silicon-compatible fabrication approach using silicon nitride waveguides fabricated in a Silicon Photonics foundry, followed by deposition of the non-standard Rare-Earth gain material outside the foundry. The latter challenge can be addressed by using higher refractive index Rare-Earth doped glass materials to enable small waveguide bending radii in order to design compact spiral amplifiers]. Aluminum oxide, with an index of 1.65 has been used for compact devices with bends as small as 80 µm for wavelengths of 1.5-µm. However, only individual devices have yet been demonstrated and we propose to take the next critical steps by incorporating such devices into silicon microsystems for the first time. We will use the IME silicon photonics offering with post-processing to achieve amplification on the silicon chip integrated with high-bandwidth modulation.

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IME SOI

Biochemical Sensor

Applications include: Environment

Medical diagnostics are critical in reducing treatment costs and improving outcomes by facilitating preventative care, early intervention, and targeted therapy. They affect 60-70% of all treatment decisions but only account for about 13% of all healthcare related costs \cite{Medical diagnose}. However, modern diagnostic tools, like enzyme-linked immunosorbent assay (ELISA), still require trained operators and secondary amplification steps with complex logistics and information management for data analysis \cite{problem3}, which restricts its adoption for fast in-field testing, especially in developing countries. Silicon photonics is foreseen to be tomorrow's main technology for the high-speed telecommunication and datacenter markets. Massive investments are being made throughout the world to boost fundamental and applied research and enable mass production at low cost. Silicon photonic biosensors have attracted increasing attention in the past 10 years due to their potential to be used for environmental monitoring, biothreat-associated agent detection, healthcare and basic biomedical research [4]. Nowadays, by leveraging the low-cost mass-production of CMOS foundries, these biosensors have recently become competitive in terms of fabrication cost. But most importantly, they will be able to address the urgent need for Point-of-Care and personalized medicine, including in remote and low-resource settings worldwide. Recently, we have successfully developed a system-level architecture based on photonic-electronic (i.e. active) chips allowing a single optical input to be distributed to multiple microring resonators (MRRs), each one individually monitored by an on-chip germanium photo-detector (PD). Silicon dies of only 1 mm2, but integrating 16 independent MRRs and PDs were fabricated through a multi-project wafer service in a CMOS foundry. Moreover, we have adapted fan-out wafer-level-packaging (FOWLP) to a lab-scale process.

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IME SOI

Biochemical Sensors

Applications include: Environment, Health/Biomedical

Silicon photonics is foreseen to be tomorrow's main technology for high-speed telecommunication and data centres. Biosensing applications have also been investigated in the past 10 years, mainly to improve their sensitivity. These biosensors have recently become competitive in terms of fabrication costs and sensitivity. Most importantly, they will be able to address the urgent need for Point-of-Care and personalized medicine.

Over the last 7 years, our team has been focusing on improving the sensitivity of ring and disk resonators biosensors. More recently, we started to develop the system-level aspects, such as chip architecture, packaging, optical/electrical interconnect, read-out electronics and instrumentation of off-the-shelf affordable lasers. In collaboration with Luxmux Technology Corporation, Calgary, we are developing a completely new biosensor platform based on 1-3 mm square dies integrating on-chip germanium photo-detectors (PDs). As a comparison, the only commercialized platform (Genalyte, US) is purely passive and relies on scanning free-optics and rather large dies (~20 mm square), which is well suited for laboratory analyses, but not for in-situ monitoring. In the mid-term, our approach also paves the way toward higher integration level, such as CMOS-photonics co-design and on-chip lasers. Having on-chip PDs also allows to relax the optical alignment tolerances, thus making the packaged sensor die easy to integrate into a compact, robust and affordable read-out system. A lab-scale Fan-Out Wafer-Level-Packaging technique has recently been tested successfully at UBC on 1 mm2 CMOS dies. We will also use the recent upgrade to 193 nm DUV lithography to explore more advanced devices. such as slot waveguides, polarization diversity resonators and develop devices at lower operating wavelengths. On the system-level side, we will develop on-chip optical filters, giant grating couplers and vertical cavity laser (VCSEL) for flip-chip integration.

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IME SOI

CMOS Compatible III-V/Si Hybrid Laser Stabilizer

Applications include: ICT

We propose to design and implement a full system comprising of an electronic-photonic circuit that will stabilize a hybrid III-V/Si laser, which will allow for its integration onto a standard silicon photonics platform. Integration onto standard silicon photonics platform is the key to high-volume low-cost production, since this will leverage the available technology that uses silicon-based platforms for manufacturing electronic circuits, and reduce the power consumed by lasers.

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IME SOI

Fabrication of Avalanche Photodector on a Silicon-on-Insulator Platform

Applications include: ICT

Detector responsivity, efficiencies, gain-bandwidth product, noises, etc. will be tested. Equipment such as lasers, probe station, high speed oscillscope, etc. are available at the PI, his collaborators' facilities and through equipment loan from CMC. The test takes approximately 1-2 months.

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IME SOI

Flex-Processing of Silicon Photonic Circuits using Integrated Micro-platforms

Applications include: ICT

This design will permit the prototyping of devices and systems that will rely on the newly developed Flex-Process, (currently under patent application via McMaster University). Flex-P permits flexible strategies for local processing of silicon photonic circuits; including the integration of detectors and amplifiers, and the trimming of resonant structures post-process. This design will include high-speed modulators trimmed to work on the ITU grid; with integrated detectors, and integrated amplifiers formed post-process. Success will allow a commercially important, high-profile technology to be disseminated.

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IME SOI

High-Q Micro-Trench Cavity Light Sources for Silicon Photonics

Applications include: Health/Biomedical, ICT

Integrated light sources are a primary challenge in silicon photonic microsystems. With this design we aim to develop a new economic and scalable approach to lasers and nonlinear optical light sources on silicon using low loss undoped and rare-earth-doped thin films. The thin films will be deposited via post-processing into novel micro-trench cavity structures to be fabricated on the AMF run. These ultra-compact and efficient microcavity light sources will have a high impact in high-speed optical communications systems. The high-Q microcavity structure to be investigated is also of interest for integrated sensing circuits.

McMaster University
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IME SOI

Integrated Coherent Transceivers

Applications include: ICT

Following the encouraging results obtained from our previous designs of traveling-wave modulator in an I&Q configuration, this new design focuses on coherent transceivers with more complex functionalities, such as polarization multiplexing and novel driving scheme, for even higher transmission rates.
Three configurations are examined in this design: 1) DP single-drive push-pull I&Q modulator, 2) DP dual-drive push-pull I&Q modulator, 3) I&Q modulator using segmented electrodes, and 4) a dual polarization coherent receiver. The first device (DP single-drive push-pull I&Q modulator) has a 4mm phase shifter and is designed for a wide E-O BW of higher than 35GHz. The second device (DP dual-drive push-pull I&Q modulator) applies a different driving configuration for a has a lower Vpi compare to its single drive counterpart (the first device) to be compatible with low-cost CMOS drivers. It has a phase-shifter of 3.9 mm. The third device compromises 4 segments, which is designed to implement more complex modulation format, such as PAM-64 and PAM-256 without using an electrical DAC. Finally, a dual polarization coherent receiver is also designed to present a monolithically integrated silicon photonics (SiP) coherent transceiver on a single chip.

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IME SOI

Integrated Optical Cavity Sensors for Mechanics

Applications include: Health/Biomedical (Experimental Physics)

Photonic waveguides and detectors with nanomechanical structures in a close proximity.

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IME SOI

Large-scale Silicon Photonic Receiver and Switch

Applications include: ICT

We propose the following Silicon Photonic Circuits:
(1) A CWDM-PDM Silicon Photonic Receiver with automated wavelength tuning and polarization stabilization;
(2) Scalability of silicon photonic switches – A photonic-electronic co-design and integration approach;
(3) Polarization-Insensitive Ring Receiver and Optical PAM-4 Ring Modulators;
(4) CWDM multiplexer/de-multiplexer using contra-directional polarization-rotating Bragg-grating add-drop filters and Polarization-Insensitive wavelength de-multiplexer using Multiple Mach-Zehnder Interference;
(5) On-chip dynamic source feedback isolation method for laser stabilization;
(6) Low-cap Photodetector

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IME SOI

Mach-Zehnder Interferometer based on Bent Contra-Directional Coupled Ring Resonators

Applications include: ICT

We propose a microring-assisted Mach Zehnder Interferometer (RAMZI) that integrates microring resonators (MRRs) with bent contra-directional couplers (CDCs) in an MZI to create a modulator where phase modulation is achieved by electrically shifting the phase response of the MRR. The design suppresses the amplitude responses of the MRR and prevents the amplitude modulation that typically accompanies detuning the MRRs. We also propose a multichannel single-side band (SSB) filter which can be used for multichannel SSB signal generation in WDM systems.

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IME SOI

Novel Integrated Hybrid Optical Waveguides and Devices for All-optical Networking

Applications include: ICT (Optical Telecommunications)

This design will prepare a foundation for the development of a novel category of highly nonlinear hybrid silicon waveguide devices. These hybrid waveguides will lead to devices enabling wavelength conversion with low optical power and possibly simplify and accelerate the treatment of optical data. These photonic devices are of great interest for ultrafast all-optical networking, which are based on keeping the data signal entirely in the optical domain from source to destination. Our goal is to design a hybrid waveguide by incorporating highly nonlinear materials such as MALH (methylammonium lad halide) perovskite or crystal violet with silicon slot waveguides to enhance the nonlinear response at telecommunication wavelengths, which will lower the power required to observe nonlinear phenomena. Moreover, we hope to overcome the limitations of silicon nanowaveguides by avoiding the nonlinear loss caused by two-photon absorption in silicon at the wavelengths of interest. The slot waveguide configuration generates high optical field intensities in the slot, which enhances nonlinear interactions with the material deposited in the slot. The design will consist of an array of silicon slot waveguides of different length and slot width. This design will also contain slot waveguide ring resonators, Y-splitter and MZI to demonstrate basic nonlinear processing with the novel waveguides including wavelength conversion, frequency comb generation and sensing.

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IME SOI

Photonic Integrated Switches for Scalable Networks

Applications include: ICT

The design is an 8-port integrated multistage network using Mach-Zehnder Interferometer (MZI) based switches. The 2x2 MZI is the building block. A Benes topology is achieved using several of the building blocks. Monitoring of the propagating optical signal inside the integrated switch is included using couplers to photodetectors. The MZI used pin doped structure for fast switching (< 10 ns).

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IME SOI

Programmable Microwave Photonic Signal Processor on a Silicon Photonic Chip

Applications include: Defence (Safety, Security), ICT

The objective of the project is to design, fabricate and evaluate a programmable photonic signal processor on a silicon photonic chip for microwave signal processing. The programmable processor has a two-dimensional mesh network structure with multiple input and multiple output ports. In each mesh cell two identical thermally tunable high-Q microdisk resonators (MDRs) are used for routing and processing the optical signal, and a low-loss waveguide crossing is employed to allow simultaneous processing optical signals. The MDR is designed to incorporate an additional slab waveguide to wrap the disk and bus waveguide, which is of help in increasing the light confinement capacity, and a micro-heater is placed on top of the disk for thermal tuning. By programming the bias voltages applied to the MDRs, the processor could be reconfigured to perform diverse signal processing functions including spectral filtering, phase shifting, temporal integration, temporal differentiation, Hilbert transformation, pulse shaping, frequency discrimination, tunable true time delay, and phased array beamforming. The device has the key advantages including strong reconfigurability and parallel computing with a low power consumption.

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IME SOI

Rare Earth Amplifiers and Tunable Lasers on a Silicon Photonic Platform

Applications include: ICT

Light emission and amplification are two primary challenges in silicon photonics. With this design we aim to develop a new economic and scalable approach to optical amplifiers and lasers on silicon using rare-earth-doped thin film technology. These ultra-compact and efficient amplifiers and lasers will have a high impact in emerging high-speed optical communications systems.

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IME SOI

Rare-earth Doped Chalcogenide Laser on the Silicon-on-Insulator Platform

Applications include: Natural Resource/Energy

This project aims to develop a laser on the silicon-on-insulator (SOI) platform by integrating rare-earth doped chalcogenide (ChG) glass as a gain medium embedded in a novel hybrid waveguide geometry. The glass will be deposited through a single-step post-process, while the etched silicon layer will provide guiding and optical feedback. We will examine the performance of a DBR laser cavity emitting at 2.0 microns.

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IME SOI

Silicon Photodetector for 850 nm Wavelength Applications
Applications include: ICT

Optical interconnects based on 850 nm wavelength directly modulated vertical cavity surface emitting lasers (VCSELs) are widely used in data centers and supercomputing systems. Silicon with high absorption coefficient at short wavelengths enables monolithic integration of an optical receiver with a photodetector reducing the complexity of the packaging. The design is a novel high-speed all-silicon photodetector operating at 850 nm with enhanced responsivity by horizontally redirecting the incident light using a grating coupler.

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IME SOI

Silicon Photonic (SiP) Circuits Development
Applications include: ICT

In support of the exponential growth of bandwidth demand, we recently reported several silicon photonic (SiP) traveling wave Mach-Zehnder modulators (TWMZMs) enabling up to 100 Gb/s transmission using pulse amplitude modulation (PAM). In our systems work, we demonstrated several record breaking single and dual polarization PAM experiments using direct detection receivers. The objective of the proposed designs is to develop system level designs targeting coherent applications, 400G optical interconnects, and low-cost coherent receivers for passive optical networks. Also, other devices will be studied as a part of the process design kit development (PDK). The circuits being proposed have not been built in a SiP platform and if successful would be extremely valuable to the SiP community. The probability of success is high because we employ known good (i) SiP device designs, and (ii) digital signal processing algorithms.

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IME SOI

Silicon Photonics Biosensors

Applications include: Environment

The recent advances in silicon photonics has led to the development of a myriad of biosensing mechanisms, such as ring resonators, interferometers or photonic crystals. The best devices reach sensitivities that compete, if not exceed the ones of gold standard techniques, such as Surface Plasmon Resonance. Surprisingly, at the best of our knowledge, only one company (Genalyte, US) commercializes silicon photonic biosensors for micro-array analysis. In collaboration with Luxmux technology Corporation, Calgary, we are developing what could be the first transportable and affordable silicon photonic product enabling the real-time detection of different biochemical species in water for quality/safety controls.

Our proposed system uses a new architecture developed at UBC based on active silicon photonic devices. The use of on-chip photo-detectors (PDs) leads to a significant decrease in the silicon biochip size, down to 1 mm square, while maintaining a high level of multiplexing, i.e. several sensing areas per chip, via microfluidic channels. PDs also simplify the optical set-up since only optical inputs are needed, thus relaxing alignment tolerances. This strategy leads to lower fabrication cost, thus paving the way to mass production of affordable biosensors (about $1 each for large volumes). A successful packaging technique for tiny chips have been developed at UBC during the past year (already tested on CMOS chips). Compatible with mass fabrication, this should also strongly lower the cost. We will also use the recent upgrade to 193 nm DUV lithography of IME to explore more advance biosensing devices. This include slot and multi-slot waveguides, sensing devices operating at lower wavelengths than the typical C-band in order to reduce water absorption losses, on-chip filters, diodes used as temperature sensing devices, thin waveguides (150 and 90-nm thick) and vertical cavity laser (VCSEL) flip-chip integration..

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IME SOI

Silicon Photonic Integrated Arbitrary Microwave Waveform Generator

Applications include: Defence (Safety, Security)

The objective of the project is to realize a fully silicon photonic integrated arbitrary waveform generator (AWG) on chip. It utilizes high-Q factor microdisk resonators to achieve high spectrum resolution (narrow to 2 GHz) and large time delay multiple-channel tunable delay lines. Thanks to the high resolution of the multiple-channel tunable delay lines, the required spectrum width of the light source is much smaller. The reduced spectrum makes it possible for the implementation of an on-chip optical frequency comb (except the tunable laser source) to realize the photonic-assisted AWG. The optical comb generator is implemented using two cascaded disk modulators and one phase modulator. The generated comb lines are sent to the tunable delay lines to adjust the time delay, the magnitude and phase. All comb lines at the outputs of the delay lines are coupled to a single waveguide and applied to a photodetector (PD) to generate a targeted microwave waveform. The system has the key advantages including high precision, wide bandwidth, flexible reconfigurability, small size and low power consumption.

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IME SOI

Silicon Photonic Networks for Reconfigurable Analog Processing

Applications include: Defence (Safety, Security), ICT

We are designing a number of test systems to implement reconfigurable analog operations using silicon photonic devices. Applications include high efficiency computing, security, and radio frequency communications. We will also continue our development of monolithically integrating electronic components into the IME platform, including operational amplifiers and bipolar transistors. Primary objectives include:

- testing and development of neural-network inspired photonic processing systems
- Circuits for optical steganography and cryptographic key generation
- Small-scale optoelectronic logic systems
- PN-doped bipolar transistors for operational and transimpedance amplification

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IME SOI

Tunable Fast Wavelength Selector

Applications include: ICT

Our submission of a silicon photonic circuit design is for a fast wavelength selector for applications in a Wavelength Division Multiplexing communication system. The function of the wavelength selector is to dynamically select any channel wavelength from input multiwavelength light source in the C-band. The technical challenges addressed in the design are to achieve tunability (or wavelength selection) across the C-band, and to minimize circuit latency in switching from one wavelength to the next. We aim to achieve an average wavelength selection speed in the range of tens of nanoseconds, with the worst case not exceeding 1 microsecond. The function of the switch is to select the drop wavelength from one of the two drop filters and switch it to the output port of the circuit. Since it is not possible to achieve fast thermo-optic tuning on a time scale of nanoseconds or tune a Si microring filter (MR filter) across the C-band using free carrier dispersion, we propose to combine the two mechanisms to achieve both fast and wideband tuning. In the proposed circuit, a 1x2 beam splitter (BS) is used to divide the incoming WDM wavelengths into two streams, which are fed to two separate tunable drop filters (DFs). The MR filters can select any wavelength in the C-band by thermo-optic tuning. The outputs of a pair of MR filters, one from each filter bank, are then combined through a 2x1 MZI switch, which is used to switch the signal from either filter to the output. We aim to achieve a switching time of less than 10 ns for the pin MZI switch. At any instant in time, only one filter in each pair will be "on" (selected) and the other will be "off". The wavelength selection time can be reduced by pre-tuning the "off" filter to the desired wavelength and then switched to the output when required. The switching time, in this case, is determined by that of the fast MZI switch, which will be within 10 ns.

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IME SOI

Tunable optical add-drop multiplexer

Applications include: ICT

The objective of this project is to develop an integrated tunable optical add-drop multiplexer (TOADM). Dynamically allocating the desired optical network resources, TODAM is a crucial device for telecommunications systems, especially in the context of metropolitan optical networks. Conventional TODAMs are implemented using discrete optical components and thus bulky and costly. Integration of various components on a single chip may drastically reduce the power consumption and footprint. Our proposed TODAM (schematic show in the attachment) consists of cascaded thermally tunable optical filters, tuning mechanism, and feedback control circuits. We will address some critical challenges in silicon photonics such as polarization diversity and sensitivity to temperature and fabrication variations. Variations of crucial components will be also designed for the purpose of calibration and future optimization.

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IME SOI

Wavelength-scale Hybrid Plasmonic Biredirectional WDM Transceivers

Applications include: ICT

The design integrates plasmonic modulators and photodetectors to high index contrast dielectric silicon waveguides on an SOI platform. The aim is to take advantage of high quality SOI processing for low loss waveguides to make very compact microring resonators for WDM and plasmonics for compact device footprints. We will be making multi-channel transceivers and test high-speed signal modulation and reception from devices across wafers.

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IME SOI

WDM-SDM Transmitter

Applications include: ICT

This design is to integrate wavelength division multiplexing (WDM) transmitter with space division multiplexing (SDM) chip-to-fiber link. In this structure, all the modulators are driven by RF signals and thermal tuned by DC signals. This design is based on our previous fabricated modulators, such as mircoring modulators (80Gb/s) [1-3]. In this run, the design parameters of each modulator are optimized for MDM–WDM link with four WDM channels and three spatial modes to support our target output of 600Gb/s transmission while connecting two chips can realize 1.2Tb/s transmission.

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Technology: Silicon Photonics - Active Silicon on Insulator (SOI) Training 2016

Projects using NSERC CREATE Si-EPIC (Silicon Electronic-Photonic Integrated Circuits Program)
For information: http://siepic.ubc.ca

Examples:

IME SOI

- **Amplifier-free Optoelectronic Oscillator Based on Silicon-on-Insulator Platform**
  University of Ottawa | Designer: Jiejun Zhang| Professor: Jianping Yao
- **High-performance Ring Filters for Wavelength Division Multiplexing**
  Université Laval | Designer: Dominic Hould| Professor: Wei Shi
- **Integrated Optical Frequency Comb Generator Enabled by Slow-light Phase**
  McGill University | Designers: Zhenping Xing, Luhua Xu| Professor: David Plant
- **Integrated tunable Sagnac interferometers based on Linearly Chirped Bragg**
  McGill University | Designer: Zifei Wang| Professor: Lawrence Chen
- **Low-Cost Coherent Receiver for Access Networks**
  McGill University | Designers: Maxime Jacques, Md Ghulam Saber | Professor: David Plant
- **Mach Zehnder Coupled Ring Modulator**
  University of British Columbia | Designer: Anthony Park | Professor: Lukas Chrostowski
- **Microwave Photonic Link with Improved Dynamic Range Integrated on SOI Platform**
  University of Ottawa | Designer: Jishen Li | Professor: Jianping Yao
- **Rare Earth Doped Tellurium Oxide Lasers**
  McMaster University | Designer: Henry Frankis | Professor: Jonathan Bradley
- **Sub-wavelength and Narrow Silicon Photonic Waveguide Structures for Optical Amplification at 1.55µm and 2 µm**
  McMaster University | Designer: Jeremy Miller | Professor: Andrew Knights
- **Thermal Tunable Arrayed Waveguide Gratings in DWDM**
  Université Laval | Designer: Qi Han | Professor: Wei Shi
- **Tunable Multi Microwave Pulse Generation based on Sagnac Interferometer and Chirped Bragg Gratings**
  McGill University | Designer: Parisa Moslemi | Professor: Lawrence Chen

MICRO-ELECTRO-MECHANICAL SYSTEMS (MEMS)

Technology: PolyMUMPs

MEMSCAP PolyMUMPs

Binary Gas Sensor

Applications include: Environment

A novel sensing mechanism for electrostatic MEMS that employs bifurcation-based sensing and binary detection is demonstrated. It is implemented as an ethanol vapour sensor that exploits the pull-in bifurcation.

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MEMSCAP PolyMUMPs

cMUTs for Ultrasonic Non-destructive Testing

Applications include: ICT (non-destructive testing is applied for evaluating structure failures in industries ranging from aerospace to transportation)

A capacitive Micromachined Ultrasonic Transducers (CMUTs) array will be implemented with the goal of producing high resolution imaging for non-destructive testing. In a previous project also fabricated through CMC Microsystems, CMUTs with a resonant frequency of 15 MHz were successfully fabricated and tested. In this project, an optimized architecture will be fabricated that needs less actuation voltage and have a resonant frequency that is less sensitive to process variations and can achieve longer range. This will allow a better frequency matching between elements of the array and therefore a higher sensitivity and better image quality.

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MEMSCAP PolyMUMPs

Dual Level Microbolometers

Applications include: Aerospace, Automotive, Defence (Safety, Security), ICT (industrial quality assurance and non-destructive testing)

Infrared (IR) sensing has always been a hot research topic since the end of World War II due to its strategic advantage of providing night vision capacity for military personal. However, the ability to tailor this feature to be used for versatile usages, which ranged from military to high-end civilian applications such as disaster prevention, security, industrial maintenance, and automotive has made it an even more attractive topic for research. This work main objective is developing a novel design for microcantilever bolometer with capacitive readout. It will be implemented using two structural layers implemented in the PolyMUMPS surface micromachined process developed at McGill University laboratories. The novel dual-layer design puts an end to the trade-off between the number of bimaterial beams, to enhance the sensor's sensitivity, and the area of the capacitance plate, for maximizing the output voltage.

McGill University
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MEMSCAP PolyMUMPs

MEMS Micromotor for Optical Swept Filters

Applications include: Health/Biomedical

The designs proposed are related to micro-opto-electro-mechanical systems and more specifically to develop MEMS micromotors for optical micromechanical systems based swept wavelength component. The micromotor is designed to rotate an integrated polygon mirror at very high speeds inside an optical filter for an optical coherence tomography (OCT) applications. The basic design consists of stator poles that surround a circular rotor which rotates about a center bearing. The goal is to achieve optimal torque and angular velocity by fine-tuning the parameters of the design such as the number of poles on the rotor and the stator, as well as reducing friction by using a novel geometrical form for the rotor. The current designs are upgraded version of previous fabricated MEMS micromotors with modification in rotor and stator design for higher torque and smaller motor footprints.

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MEMSCAP PolyMUMPs

MEMS Transducers for Cornell/NASA

Applications include: Aerospace

Air Coupled moving membrane transducers for imaging on MARS in collaboration with Cornell/NASA

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MEMSCAP PolyMUMPs

Micromirror Display for Personalized Tailoring

Applications include: ICT (cloth tailoring)

This application is to use PolyMUMPS to fabricate 2D micromirror for laser display. Our group had successfully developed PolyMUMPS micromirror laser display with application in Head-up Display (HUD). The present application is to develop micromirror suitable for display in personalized tailoring business, which is to be in collaboration with the famous laser templating and inspection company in Canada. The micromirror laser display can project accurately the template for any desired type of clothes from a comprehensive data library according to an individual's size without depending on the skills of a tailor.

Ryerson University
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MEMSCAP PolyMUMPs

Multiple Moving Membrane MEMS Transducers

Applications include: ICT, Health/Biomedical (defects in HVDC power cables and breast cancer screening)

Air coupled multi moving membrane capacitive transducers are investigated for imaging applications.

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Technology: MicraGEM-Si™

Micralyne MicraGEM-Si™

2D Micromirror for Portable Laser Marking Machine

Applications include: ICT (laser marking industry)

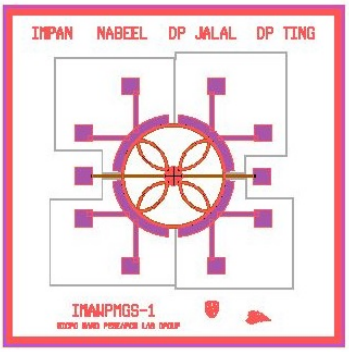
This design is to fabricate a 2D micromirror which can steer an optical beam about 2 orthogonal axes for laser marking application. The 2D micromirror is to be developed to output 2 times larger rotation angle to enlarge the marking area of the current system by 4 times without sacrificing the making speed. It will be driven by electrostatic torque and have innovative and pre-assembled fixed electrodes to enlarge the rotation angle. The 2D micromirror consists of four actuators to drive a 2D rotation plate with a mirror bonded on the top of it. Each actuator includes a lower-fixed-comb, an up-fixed-comb and a moving-comb. The up-fixed-comb is flipped up and bonded to the substrate permanently through a flipping and bonding process after all fingers are fabricated. This process first applies a high voltage between the flipping plate and the flip electrode to pull the flipping plate down and touch the flip block. Then an adhesive dispensing mechanism dispenses a Nano liter epoxy to the flipping plate and the flip block/substrate to bond them permanently. The voltage is removed after bonding. Our lab has successfully developed the technology of bonding two MEMS structure which has been used in our translating micromirror for spectrometer. It will be used in this project for the two bonding processes in the novel micromirror. When apply voltage to the lower-fixed-finger or flipped up-fixed-finger, the moving-finger rotates clockwise or counter-clockwise about its pivoting point on the left of the moving-finger. In the operation the whole finger length is used to generate electrostatic force, unlike in conventional designs only half of the finger length is used to generate electrostatic force. Thus, the new design can generate the electrostatic force/torque twice that generated in conventional designs.

Ryerson University
Designer: Hui Zuo Email: hui.zuo@ryerson.ca
Professor: Siyuan He Email: s2he@ryerson.ca

Micralyne MicraGEM-Si™

MEMS Gyroscope

Applications include: Aerospace, Automotive, Health/Biomedical



Design and development of a novel MEMS Gyroscope with high Q-factor by combining the electrostatic attraction and repulsion forces to match the drive and sensing frequencies.

University of Windsor
Designer: Imran Khan Email: khan1cm@uwindsor.ca
Professor: Jalal Mohammed Ahamed Email: jahamed@uwindsor.ca

Technology: MEMS Integrated Design for Inertial Sensors (MIDIS™) Platform

Teledyne DALSA MIDIS™

Nonlinear Coriolis Vibratory Gyroscopes (I and II)
Applications include: Aerospace, Automotive, Entertainment

Our main goal is to explore feasibility of application of well-known nonlinear phenomena in improving performance of inertial sensors particularly gyroscopes. Our objectives can be summarized as follows:

1) Design and fabrication of inertial sensors operating on the principle of 2:1 internal resonance.
2) Characterization of the sensor behavior under impact of various excitation forcing functions.
3) Design of inertial sensors based on 2:1 resonance ratio with less sensitivity to fabrication defects and imperfections.
4) Application of control systems to improve the sensitivity and internal resonance condition.
5) Investigation into packaging impact on quality factor and performance of the sensors. (Packaged chips by DALSA will help us a lot in this specific goal to achieve high quality factors).

Simon Fraser University
Designer: Fatemeh Edalatfar Email: fedalatf@sfu.ca
Designer: Atabak Sarrafan Email: asarrafa@sfu.ca
Professor: Behraad Bahreyni Email: behraad_bahreyni@sfu.ca

Technology: PiezoMUMPs

MEMSCAP PiezoMUMPS

Contour-mode Resonator (CMR)

Applications include: ICT (wireless transceiver applications)

The design includes the CMR resonators and filters based on PiezoMUMPs process. The objective is measuring the designed chips and comparing with FEM simulation results. (The project is a part of my PhD thesis which will be defended at university of Waterloo.)

University of Waterloo
Designer: Arash Fouladi Azarnaminy Email: a2foulad@uwaterloo.ca
Professor: Raafat Mansour Email: rrmansour@uwaterloo.ca

MEMSCAP PiezoMUMPS

High Performance Vibration Sensors

Applications include: Defence (Safety, Security), Natural Resource/Energy (undersea exploration)

The goal is to evaluate vibration sensor designs for two distinct applications. One application is measurement of weak, high frequency vibrations within solid structures. The second application is for underwater ultrasound detection. Our goal is to evaluate designs suited for these applications and compare them with existing industrial solutions.

Simon Fraser University
Designer: Fatemeh Edalatfar Email: fedalatf@sfu.ca
Professor: Behraad Bahreyni Email: behraad_bahreyni@sfu.ca

MEMSCAP PiezoMUMPS

High Sensitivity Gas Sensors Based on SAW Resonators and Micro Heaters

Applications include: Environment, ICT (industrial applications, environment/air quality monitoring, on demand ventilation systems, smoke detectors)
The goal of this phase of the project is to implement a combined sensor utilizing both a SAW resonator and a micro-heater to measure the frequency and resistance change at the same time, and therefore combine the advantages of both sensing mechanisms. This is expected to increase the sensor's sensitivity and selectivity, which allows the discrimination between closely related analytes, while reducing the sensor hysteresis.

McGill University
Designer: Yu Zheng Email: yu.zheng3@mail.mcgill.ca
Professor: Mourad El-Gamal Email: mourad.el-gamal@mcgill.ca

MEMSCAP PiezoMUMPS

MEMS Actuators for Reconfigurable Silicon Photonics

Applications include: ICT

We requested CMC resources to update the design for a novel electrostatic MEMS actuator integrated with movable channel waveguides on the same chip to form a 1xN optical switch. The actuator designs from the previous PiezoMUMPs run by CMC have been modified following the testing of the dies received from the previous fabrication run. The 1NX rotational actuator consists of two curved comb drives which enable rotation of an integrated waveguide, making possible the coupling of light from a movable waveguide into different waveguides on the same chip. However, the resources requested now are to demonstrate and optimize different MEMS actuators that will be integrated with the optical structures once their performance has been proven satisfactory. Electrostatic actuation achieved through the curved comb drive design is used to realise in-plane rotational motion of the suspended input beam. Moreover, an updated electrostatic latching mechanism prone to mechanical stress for "set and forget" functionality of the device will be integrated in this MEMS. This design will incorporate an electrostatically actuated gap closing mechanism that will limit the air gap between the input and the output waveguides from ~3µm to a few nm and thus minimize the optical losses associated with MEMS design constraints and fabrication limitation.

École de technologie supérieure
Designer: Suraj Sharma Email: suraj.sharma.1@ens.etsmtl.ca
Professor: Frédéric Nabki Email: frederic.nabki@etsmtl.ca

MEMSCAP PiezoMUMPS

Microelectromechanical Systems (MEMS) Integration in Micromixers

Applications include: Health/Biomedical, Environment

Many micromixers found in literature use external actuators to achieve mixing. The primary objective of this design is to miniaturize active micromixers used for microfluidics. PiezoMUMPs was chosen to show that we can cost-effectively make use of industrial MEMS technologies to achieve hybrid active and passive micromixers based on polymer and silicon technologies.

Université du Québec à Montréal (UQAM)
Designer: Simon Dallaire Email: dallaire.simon@courrier.uqam.ca
Professor: Paul-Vahe Cicek Email: cicek.paul-vahe@uqam.ca

MEMSCAP PiezoMUMPS

Multi-frequency Piezoelectric Energy Harvester

Applications include: Environment

Energy harvesting from ambient resources is recognized as an unlimited and sustainable technique for low-power electronic applications. Among available resources in the normal environment, vibrations due to ubiquitous existence in environmental and ease of trapping are known as one of the most promising harvestable resources. During the past decade, several techniques (such as electrostatic-, electromagnetic- and piezoelectric-based methods) for converting vibration to electricity have been proposed. Each technique has significantly different pros and cons in terms of portability, power density, cost effectiveness, etc. Among them, the piezoelectric-based technique has gained a lot of interest recently thanks to the deposition capability of piezoelectric materials by micromachining technology, which is able to produce MEMS-based energy harvesters featuring high degree of portability. In this study, we have proposed an array of 'T'-shaped piezoelectric cantilever in MEMS scale for converting ambient vibrations (e.g., induced by wind flow, ocean waves, etc.) to electrical power. In our previous study, performance of 'T'-shaped piezoelectric harvester, theoretically and experimentally investigated and it is found that the 'T'-shaped piezoelectric energy harvester consists of higher power density in comparison with the conventional MEMS piezoelectric harvesters. Thus, in this design we will use several 'T'-shaped cantilevers as an array, therefore power density and operating frequency bandwidth of the proposed harvester will be significantly enhanced.

Memorial University of Newfoundland
Designer: Seyedfakhreddin Nabavi Email: snabavi@mun.ca
Professor: Lihong Zhang Email: lzhang@mun.ca

MEMSCAP PiezoMUMPS

Multimode Piezoelectric Harvester with New Electrode Configuration

Applications include: Natural Resource/Energy

Energy harvesting from ambient vibration by micro-electromechanical systems (MEMS) is recognized as a practical method for powering of low-electronic consumer applications. During the last decades several attempts have been made to provide MEMS piezoelectric harvesters with applicability of operating in real environments, however, generating voltage in a narrow bandwidth is their main obstacle. Thus, in this article we propose a novel MEMS piezoelectric harvester with capability of vibrating in multi-degree-of-freedoms, whose operating bandwidth enhanced. The proposed harvester has a symmetric structure with clamped-clamped configuration and three proof masses are located in three different locations. Therefore, this uniform mass distribution enlarges the harvested voltage efficiency.

Memorial University of Newfoundland
Designer: Seyedfakhreddin Nabavi Email: snabavi@mun.ca
Professor: Lihong Zhang Email: lzhang@mun.ca

MEMSCAP PiezoMUMPS

Novel PMUT Actuation System

Applications include: Health/Biomedical

A novel actuation system for Piezoelectric Micromachined Ultrasonic Transducers (pMUTs) will be implemented. The system will make it possible to start but also to stop PMUTs on demand in order to achieve short ultrasound pulses in the time domain. This will allow to increase the axial resolution of PMUTs based imaging system.

Université du Québec à Montréal (UQAM)
Designer: Alexandre Robichaud Email: robichaud.alexandre@courrier.uqam.ca
Professor: Frédéric Nabki Email: frederic.nabki@etsmtl.ca

MEMSCAP PiezoMUMPS

Piezoelectric Harvester with New Configuration for Electrodes

Applications include: ICT (energy harvesting)

In this study, we proposed a pair of 'T'-shaped piezoelectric cantilevers in MEMS scale for converting ambient vibrations (e.g., induced by wind flow, ocean waves, etc.) to electrical power. In this regard, 'T'-shaped cantilevers are located very close each other, therefore, non-linear air damping between them, which is operated as spring softening, can improve the cantilevers oscillations. Thus, this proposed configuration has larger power density in comparison with conventional MEMS piezoelectric harvesters. The 'T'-shaped piezoelectric energy harvester consists of the three different rectangular cantilevers, which are anchored in two different area. The longest cantilever from one side is anchored to substrate therefore its anchor location cannot change during flapping. While two other cantilevers are located on free tip of the first cantilever thus, this moving point can be considered as a moveable anchor for second and third cantilevers. Consequently, these fixed and unfixed anchors in the proposed 'T'-shaped MEMS piezoelectric cantilever offers oscillation in different frequency. Thus, the proposed new mechanical structure will make the system usable for operating at various frequencies so that the efficiency of our MEMS-based piezoelectric energy harvester will keep consistent while ambient frequency is changing.

Memorial University of Newfoundland
Designer: Seyedfakhreddin Nabavi Email: snabavi@mun.ca
Professor: Lihong Zhang Email: lzhang@mun.ca

MEMSCAP PiezoMUMPS

Piezoelectric Resonator Series Arrays for Higher-quality Filtering

Applications include: ICT

Series-arraying of piezoelectric resonating devices will be investigated with the goal of improving filtering quality. The long-term objective is to subsequently transpose and adapt the most successful device designs to an in-house above-IC-compatible MEMS fabrication technology.

Université du Québec à Montréal (UQAM)
Professor: Paul-Vahe Cicek Email: cicek.paul-vahe@uqam.ca

MEMSCAP PiezoMUMPS

Piezoelectric Vibration Energy Harvester

Applications include: Environment, Health/Biomedical, ICT

Working towards an integrated energy harvesting system for sensor nodes, the proposed design is a piezoelectric vibration energy harvester consisting of cantilevers and other vibrating geometries designed to achieve low resonant frequencies, wide bandwidths and high-power outputs. New architectures to achieve these specifications have been developed and to be integrated with their power management circuit in the same package to be tested to power pressure and humidity sensors. The design aims to optimise devices validated in two previous runs to increase the energy transduction coefficient and tailor the operating frequency range to structural health monitoring applications.

Université du Québec à Montréal (UQAM)
Designer: Abdul Hafiz Alameh Email: alameha@hotmail.com
Professor: Frédéric Nabki Email: frederic.nabki@etsmtl.ca

MEMSCAP PiezoMUMPS

Strain Sensor Based on Resistive and Displacement Method

Applications include: Aerospace (and others)

The goal is to design a novel type of MEMS strain sensor that will be integrated with an embedded system to have complete strain sensor system. Different MEMS structures based on contact resistances will be investigated to find the most suitable for strain sensor applications. Test structures will be fabricated to generate an accurate model of a Si-Si contact resistance that will be used for further designs. The design will allow to measure displacement from 2µm to 25µm.

Université du Québec à Montréal (UQAM)
Designer: Philippe-Olivier Beaulieu Email: philippe-olivier_beaulieu@hotmail.com
Professor: Frédéric Nabki Email: frederic.nabki@etsmtl.ca

MEMSCAP PiezoMUMPS

The Wideband MEMS Energy Harvester Utilizing Nonlinear Springs

Applications include: Environment

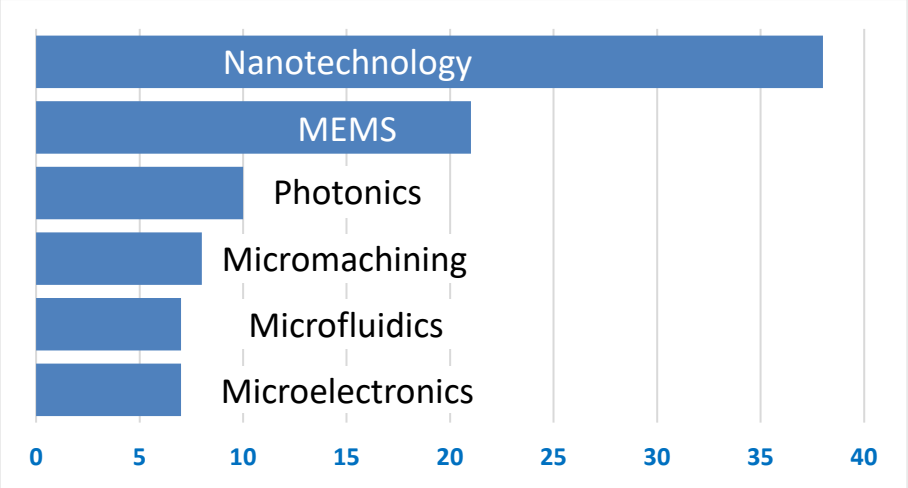
Energy harvesting from ambient resources is the key of providing an unlimited and sustainable power supply for electronic consumer applications. Among available resources in the normal environment, vibrations due to ubiquitous existence and ease of trapping are known as one of the most promising harvestable resources. During the past decade, several techniques (such as electrostatic-, electromagnetic- and piezoelectric-based methods) for converting vibration to electricity have been proposed. Each technique has significantly different pros and cons in terms of portability, power density, cost effectiveness, etc. Among them, the piezoelectric-based technique has gained a lot of interest recently thanks to the deposition capability of piezoelectric materials by micromachining technology, which is able to produce MEMS-based energy harvesters featuring high degree of portability. In this study, we proposed a pair of 'T'-shaped piezoelectric cantilevers in MEMS scale for converting ambient vibrations (e.g., induced by wind flow, ocean waves, etc.) to electrical power. In this regard, 'T'-shaped cantilevers are located very close each other, therefore, non-linear air damping between them, which is operated as spring softening, can improve the cantilevers oscillations. Thus, this proposed configuration has larger power density in comparison with conventional MEMS piezoelectric harvesters.

Memorial University of Newfoundland
Designer: Seyedfakhreddin Nabavi Email: snabavi@mun.ca
Professor: Lihong Zhang Email: lzhang@mun.ca

MNT (Micro-Nano Technology) FABRICATION

CMC's MNT Portal - www.cmc.ca/MNT - includes more than **40** MNT facilities located at universities across Canada offering mask generation, etching, materials deposition, lithography, and characterization.

Projects that benefited from CMC's MNT Portal financial assistance and concluded in 2017/18:



Examples:

MNT: MEMS

- **A CMUT Array Based on Annular Cell Geometry for High-Intensity Focused Ultrasound (HIFU) Therapeutic Applications** | Lab: The Giga to Nanoelectronics (G2N)
  University of Waterloo
  Designer: Shuai Na | E: s2na@uwaterloo.ca
  Professor: Tze-Wei (John) Yeow | E: jyeow@uwaterloo.ca

- **2D Crystals in Microwave MEMS Circuits: sensors, materials studies, and approaching quantum limits** | Lab: NanoFabrication Kingston (NFK)
  Queen's University
  Designer: David Northeast | E: dnortheast@physics.queensu.ca
  Professor: Robert Knobel | E: knobel@queensu.ca

MNT: Microelectronics

- **Design Principles for Organic Electrochemical Transistors** | Lab: 4D LABS
  Simon Fraser University
  Designer: Parisa Shiri | E: pshiri@sfu.ca
  Professor: Loren Kaake | E: lkaake@sfu.ca

- **WO3 Thin Films (Photo)transistors Interfaced with Aqueous Electrolytes** | Lab: GCM Lab
  Polytechnique Montréal
  Designer: Martin Schwellberger-Barbosa | E: martin_s_barbosa@hotmail.com
  Professor: Clara Santato | E: clara.santato@polymtl.ca

MNT: Microfluidics

- **Developing a Nanofluidic Device for Controllable Nanopore-based Molecular Sensing** | Lab: McGill Nanotools Microfab (MNM)
  McGill University
  Designer: Zhiyue Zhang | E: zhiyue.zhang@mail.mcgill.ca
  Professor: Sabrina Leslie | E: sabrina.leslie@mcgill.ca

- **Microfluidics for Localized Stimulation of Axon for Collateral Branching Studies in ALS** | Lab: nanoFab Centre
  University of Calgary
  Designer: Hamid SadAbadi | E: hamid.sadabadi@ucalgary.ca
  Professor: Amir Sanati Nezhad | E: amir.sanatinezhad@ucalgary.ca

MNT: Micromachining

- **3D Innervated Tissue On-chip for the Study of Spinal Cord Injuries (SCI)** | Lab: Microsystems Hub
  University of Calgary
  Designer: Sultan Khetani | E: sultan.khetani@ucalgary.ca
  Professor: Amir Sanati Nezhad | E: amir.sanatinezhad@ucalgary.ca

- **Wearable CMOS Ultrasound Transducer for Continuous Monitoring of Red Blood Cell Aggregation** | Lab: GCM Lab
  Polytechnique Montréal
  Designer: Khaled Younes | E: khaled.abdel.latif.younes@umontreal.ca
  Professor: Frédéric Lesage | E: frederic.lesage@polymtl.ca

MNT: Nanotechnology

- **Creation of Dynamic Exciton-Polariton Lattices for Quantum Simulators** | Lab: Quantum NanoFab (QNF)
  University of Waterloo
  Designer: Mats Powlowski | E: mspowlow@uwaterloo.ca
  Professor: Na Young Kim | E: nayoung.kim@uwaterloo.ca

- **Fabrication of Fused Silica Microlens Arrays** | Lab: Advanced Materials and Process Engineering Laboratory (AMPEL)
  University of British Columbia
  Designer: Sam Park | E: hongbae@ece.ubc.ca
  Professor: Boris Stoeber | E: stoeber@mech.ubc.ca

MNT: Photonics

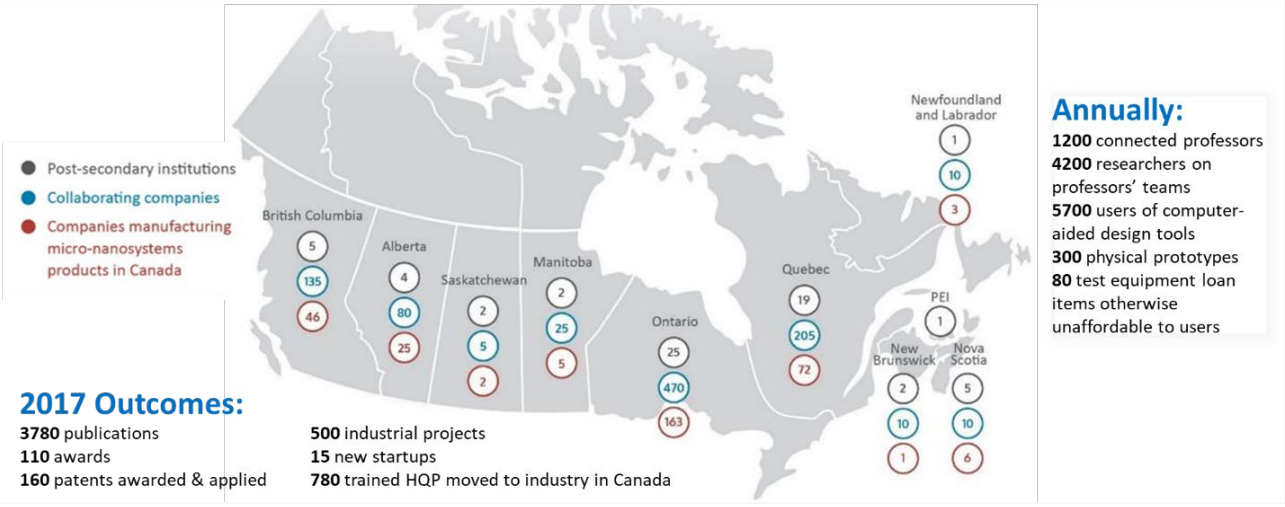
- **Ultra-High-Efficiency Ultra-Thin-Silicon Photonic Crystal Solar Cells** | Lab: Toronto Nanofabrication Centre (TNFC)
  University of Toronto
  Designer: Rajiv Prinja | E: rajiv.prinja@mail.utoronto.ca
  Professor: Nazir Kherani | E: kherani@ecf.utoronto.ca

- **High Speed and High Output Power Uni-traveling Carrier Photodiode** | Lab: Laboratory of Micro and Nanofabrication (LMN)
  Concordia University
  Designer: Jie Xu | E: x_jie12@encs.concordia.ca
  Professor: John Xiupu Zhang | E: xzhang@ece.concordia.ca

Appendix A1 – CMC Microsystems and Canada's National Design Network®

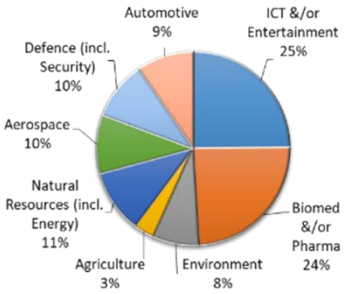
2017/18:

A Canada-wide collaboration between 66 universities/colleges to connect 10,000 academic participants with 950 companies to design, make and test micro-nanosystem prototypes. CMC manages Canada's National Design Network.



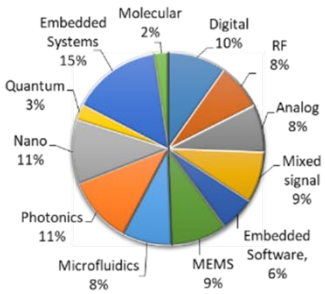
CNDN Academic Landscape 2017/18:

Technology Application



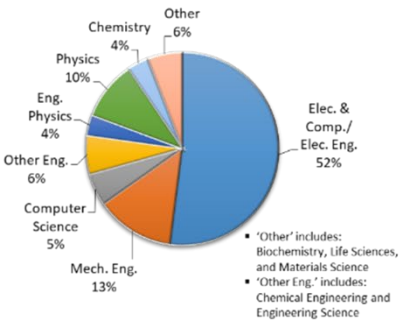
# of professors = 1117
# of interests = 3079

Design-Oriented Interests



# of professors = 1126
# of interests = 4513

Disciplines/Departments

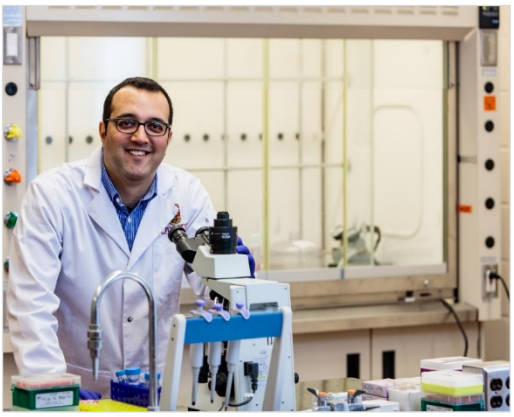


# of professors = 1209

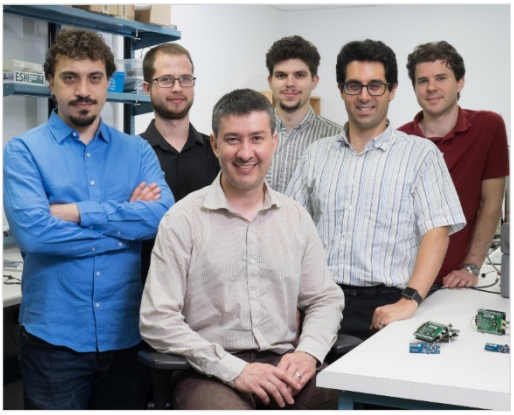
Appendix A2 – Success Stories in 2017/18

Researchers across Canada are engaging in microsystems and nanotechnology research that is resulting in excellence, commercialization, collaborations, and highly trained and qualified people. To read CMC Success Stories, including the examples listed below, see www.cmc.ca/SuccessStories.

- Channeling new approaches to assisted reproduction
  Reza Nosrati, Queen's University
  Using microfluidics and advanced microscopy, he and his colleagues are developing simple but functional technologies for analysing and selecting sperm, and ultimately improving fertilization rates. His subsequent work focused on paper-based microfluidics to identify concentration of sperm, and their motility. The device works like a pH strip, used for testing acidity or alkalinity. Their long-term plan is to pair the device with a cell-phone application that could analyse and track semen quality day to day, enabling individuals to test themselves.
  (Published April 2017)

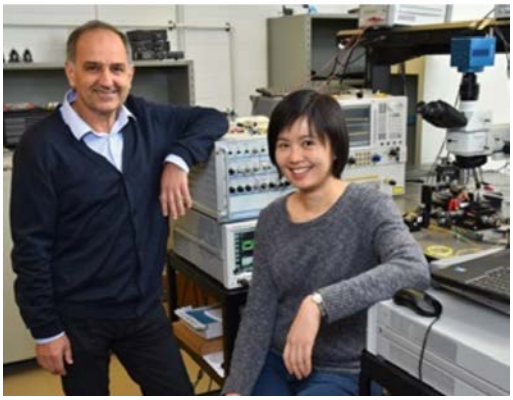


- Novel transceiver paves the way
  Frederic Nabki & Dominic Deslandes
  École de technologie supérieure
  Their company, Spark Microsystems, was selected for inclusion in ÉTS's CENTECH Propulsion program, a two-year growth acceleration program targeting high-potential companies. The company is also supported by Ecofuel, an accelerator that specializes in clean technology.
  (Published July 2017)



- Global conference recognizes made-in-Canada photonics innovations – three researchers from CNDN received "Top-Scored Paper" honours at OFC 2017
  - **Joyce Poon & Sorin Voinigescu, University of Toronto –** for development of a 3D integrated Si-P electro-optic transmitter (Active Devices)
  - **David Plant, McGill University** – for Si-P intensity modulators showing record-breaking modulation speeds (Active Devices)
  - **Lukas Chrostowski, UBC** – for a new method of automatically tuning and stabilizing high-order optical filters in Si-P. (Passive Devices)

  (Published December 2017)



Appendix B – CNDN Prototype Manufacturing Technologies

Micro- Nanoelectronics

STMicroelectronics FD SOI 28nm CMOS
TSMC 65nm GP CMOS
TSMC 65nm LP CMOS
TSMC 0.13µm CMOS
TSMC 0.18µm CMOS
TSMC 0.35µm CMOS
AMS 0.35µm CMOS - options: Standard, Opto, High Voltage, Post Processing
Teledyne DALSA 0.8µm CMOS - options: Standard Voltage, High Voltage
National Research Council Canada (NRC) Gallium Nitride (GaN)

Photonics & Optoelectronics

AMF Silicon on Insulator, Passives and Actives
Epitaxy - options:
Canadian Photonics Fabrication Centre (NRC-CPFC) III-V Epitaxy on InP Substrates
FBH-Berlin III-V Epitaxy on GaAs Substrates
Landmark III-V Epitaxy on GaAs and InP Substrates

MEMS

MEMSCAP PiezoMUMPs
MEMSCAP PolyMUMPs
MEMSCAP - Post-processing for PolyMUMPS
Micralyne MicraGEM-Si™
Teledyne DALSA MIDIS™ Platform

This chart is a representative sample of the prototyping products available to Canada's National Design Network. More information online: www.cmc.ca
Revised: *2017/2018*

For information, contact us:

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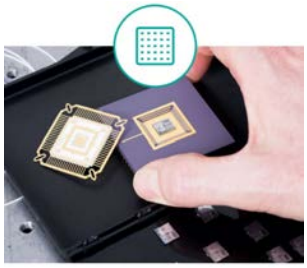
Don't hesitate to contact me about opportunities for industry and academic R&D.

www.cmc.ca



www.cmc.ca/FAB

LOWERING BARRIERS TO TECHNOLOGY ADOPTION

CMC helps researchers and industry across Canada's National Design Network® develop innovations in microsystems and nanotechnologies.

www.cmc.ca