A Process Design Kit for Superconducting Components

Niharika Kohli, Charles Paradis, Siamack V. Grayli and Udson C. Mendes
CMC Microsystems®, Canada

Introduction

In the last decade, we have observed the rapid development of superconductor-based quantum computing platforms [1,2]. Indeed, quantum computers with more than 400 superconducting qubits are now a reality [3]. The realization of quantum computers involves the integration of Josephson-junction qubits with other quantum-limited superconducting components such as readout lines and parametric amplifiers. To operate at the quantum limit, superconducting circuit components need to meet certain requirements concerning the components' physical (e.g., scale and dimension), electrical (e.g., critical current and junction capacitance) and functional characteristics (e.g., resonance frequency and coupling efficiency). Therefore, precise fabrication guidelines encompassing the component requirements, design environment, and the design rule checks are fundamental to generate a functional superconducting quantum computer device.

Fabrication guidelines are tied to a process design kit (PDK). The PDK contains not only the set of rules regarding all the required mask layers used in the fabrication process, but also a library of basic components provided by the foundry to facilitate the design process. Additionally, the PDK environment provides automated design rule checking (DRC) to ensure that the foundry rules are not violated. For example, it includes rules for checking the minimum width allowed for a specified layer or the spacing between two different layers. The PDK library of components provides reference designs and/or parameterized cells (P-cells) to help designers build their layouts in a time-efficient manner. PDKs have more components in them, but the focus of this paper will be on the P-Cells, or layout devices. PDKs have existed for the standard semiconductor industry for many decades.

In this white paper, we provide a brief overview of a superconducting component PDK built in Siemens L-Edit [4] for STAR Cryoelectronics' fabrication process [5]. We start by providing a brief overview of different superconducting devices, followed by a description of the L-Edit and discuss how to perform DRC using Calibre within L-Edit. Next, we present various CMC Microsystems® reference design cells, both fixed and automated, created for STAR Cryoelectronics' fabrication process. Finally, we discuss how to perform automated routing using Coplanar Waveguides (CPW) in L-Edit.

Superconducting devices

Superconducting devices are made from materials that become superconducting at low temperatures. Superconductivity refers to the material's capability to conduct electrical current without resistance [6]. Examples of superconducting devices include Josephson junctions, CPW, superconducting quantum interference devices (SQUIDs), and resonators. Josephson junctions, formed by two superconducting metals, such as aluminum or Niobium, separated by a thin insulator layer, are ubiquitous in today's superconducting quantum technology. Indeed, Josephson junctions are used to create qubits and Josephson parametric amplifiers. CPWs are a transmission line architecture that places a ground plane on both sides of a central conducting line, all made of a superconducting metal. The CPW frequency modes and impedance are controlled by the central line width as well as the width of the gaps between the central line and the ground planes. SQUIDS are made from two Josephson junctions placed in parallel. A SQUID can be used as a variable non-linear inductance whose value is controlled by the junction's critical current. As for the resonators, they consist of a specific length of waveguide that is usually a quarter or a half of the wavelength associated with the desired resonator frequency. The main device of interest in the field, a qubit, is a two-level system that can be used as a basis for quantum computing applications. One such qubit, called a transmon, is made from a Josephson Junction connected in parallel with a large capacitor, thus creating a fixed-frequency qubit. A flux-tunable qubit frequency can be obtained using a SQUID geometry to form the transmon qubit [7]. In the remainder of the article, we present how these devices can be designed with L-Edit.

L-Edit Description

The L-Edit layout editor provides an efficient and easy way to use a platform for designing layout for various technologies such as integrated circuits, Microelectromechanical systems (MEMS) and Photonics [4]. L-Edit is available via CMC cloud for academics or Start-ups participating in the Virtual Incubator Environment [8]. In this paper, we discuss how L-Edit can be used to design superconducting components in STAR Cryoelectronics' fabrication process used in the world's first superconducting MPW service organized by CMC.

This section provides a brief introduction to the L-Edit layout editor. Figure 1 shows L-Edit's main window and the red boxes mark some of its most used features. These features are as follows:

1) Main toolbar: Used to open and save designs through the "File" tab. Other tabs like "Cell" let the user open a new cell view to add a new layout to the library. It also has a "Help" tab to find more detailed information on several topics.
2) Drawing toolbar: Used to add new objects like boxes, polygons, wires, and circles in the layout. The first tab with an arrow [] lets the user select a particular object on the layout and is used frequently in the design.

3) Editing toolbar: Used for functions such as copying, rotating, and flipping of a selected object.
4) Current layer: This shows the layer selected on the layer palette. Any object added to the layout will be drawn on this selected layer.
5) Layer Palette: Consists of all the PDK layers which are fabricated by the foundry and can be used by the designer for layout. The right-most column shows the GDS (Graphic Design System) number of layers to identify the layer (mask) in the exported GDS.
6) Current cell: Is the cell view currently open in the tool. For example, in this figure a cell named "Die_outline" is open in the layout window.
7) Libraries: This tab can be selected to view all the libraries in the PDK.
8) Verification Navigator: Provides the results of the DRC after the DRC is run in the tool.

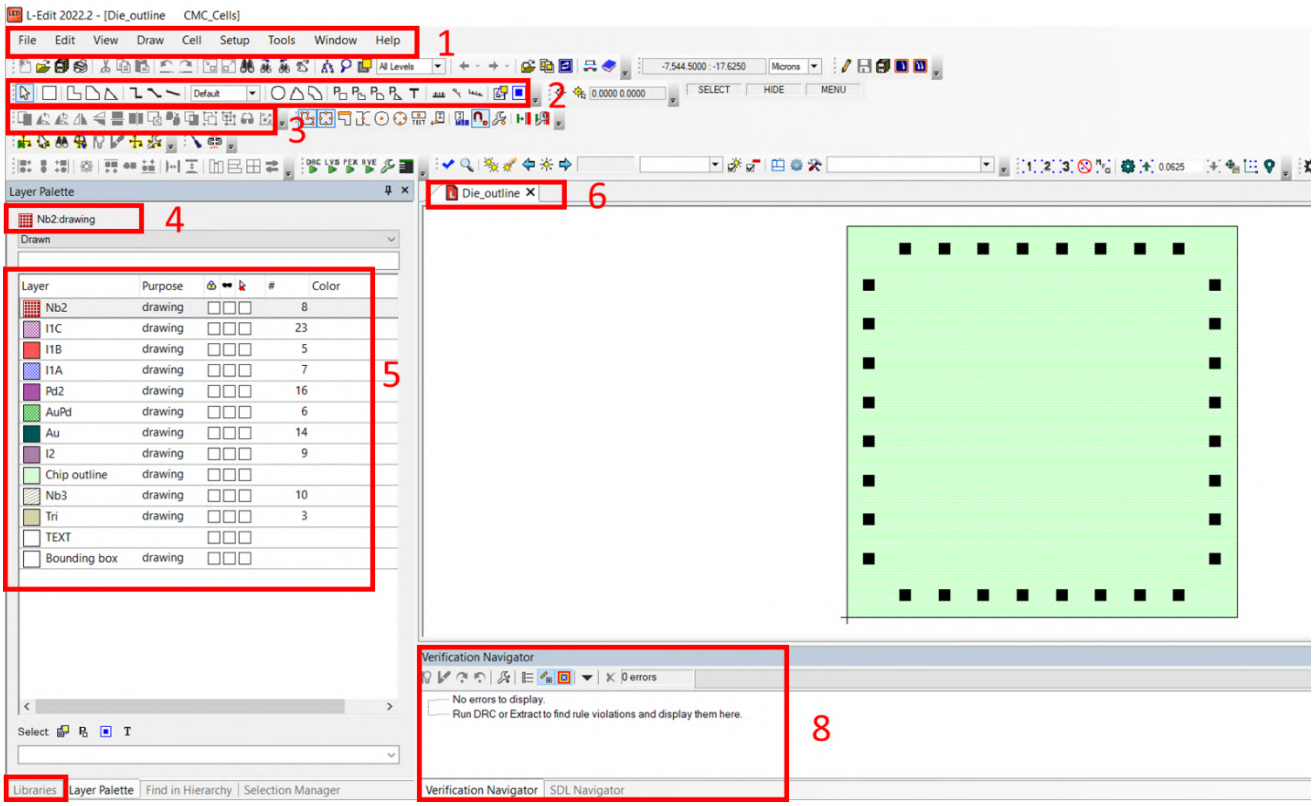

Figure 1: L-Edit main window and useful features such as Main (1), Editing (2) and Drawing toolbars (3), Current layer (4), Layer Palette (5), Current cell (6), Libraries (7) and Verification navigator (8).

A more detailed description of the various features can be found in the tool manuals that can be accessed directly from the 'Help' menu.

Verifying the Manufacturability of the Process Design Kit

The PDK contains a set of design rules provided by the foundry. It allows consistent and reliable fabrication of the designed layouts. Moreover, the PDK enables automated Design Rule Checking of the design layout. The DRC is a crucial step in the design process, as it permits us to verify any violation of the fabrication rules. Calibre is Siemens' design-rule checker. To run Calibre, in L-Edit, the designer must simply go to Tools → Calibre or click the DRC tab [ ] on the toolbar. The results of the DRC showing violations of the foundry fabrication rules are displayed in the Verification Navigator (Fig. 1 red box 8). The layout rule violations can be selected one by one, and modifications can be made to "clean" the design. Once the DRC is completed on the individual cells, then the PDK is ready for production use.

CMC reference designs

A library of basic component reference designs, named "CMC_Cells," is included in the PDK. The library guides the designer to draw layouts of various superconducting circuit elements. These are either layout cells or P-cells, we present some examples below. There is also an option to do automated routing using CPWs and bends, which is also discussed at the end of the section.

1 Layout cells

Layout cells are designed for specific dimensions and the designer can manually change these dimensions according to their design needs. For example, the PDK consists of layout cells for Josephson junction, resistors, contact pads, among others.

- The "Circular junction" cell consists of a circular Josephson junction and circular vias. Vias are used to connect the junction's top and bottom electrodes to the metal layer, as depicted in Fig. 2(a).
- The "Resistor" cell consists of a block of the resistor layer from the PDK. The resistor, a green rectangle, is directly connected at both ends to the metal (red rectangles) as illustrated in Fig. 2(b).
- The "Pad" cell, shown in Fig. 2(c), consists of a stack of all the layers, allowing for the connection of external inputs and outputs to the elements of the circuit.

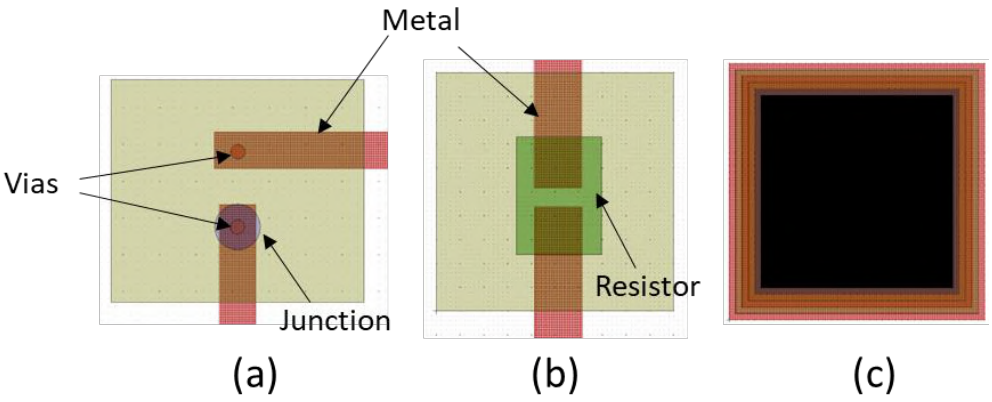

Figure 2: Examples of reference layout cells: a) circular Josephson junction, b) resistor, and c) pad.

2 P-cells

The PDK also includes various parametrized cells (P-cells), in which parameters, such as width and radius, can be automatically adjusted according to design specifications. In L-Edit, P-cells can be simply dragged and dropped from the CMC_cells library onto the layout window and a "parameter window" pops up. The user can adjust P-cell parameters in this window. The use of P-cells saves time for the designers by eliminating the need to draw them manually.

In the following text, we present a few P-Cell examples such as inductors, CPWs and bends, and fingered capacitors.

- As illustrated in Fig. 3(a), both spiral and square inductors P-cells are available. The designer can automatically update the width of the metal, radius, and number of turns.
- P-cells for Finger capacitors, Fig. 3(b), are also available in the PDK. To design capacitors of a desired capacitance value, parameters such as finger length, width, spacing, number of fingers can be easily modified in the parameter window.
- CPW waveguides and bends, as depicted in Fig. 3(c), are also provided in the PDK. These P-cells can be used to design, for example, superconducting transmission lines or CPW resonators. The width, spacing and radius of the central line and the outer ground plane can be modified to achieve a desired mode frequency and characteristic impedance.

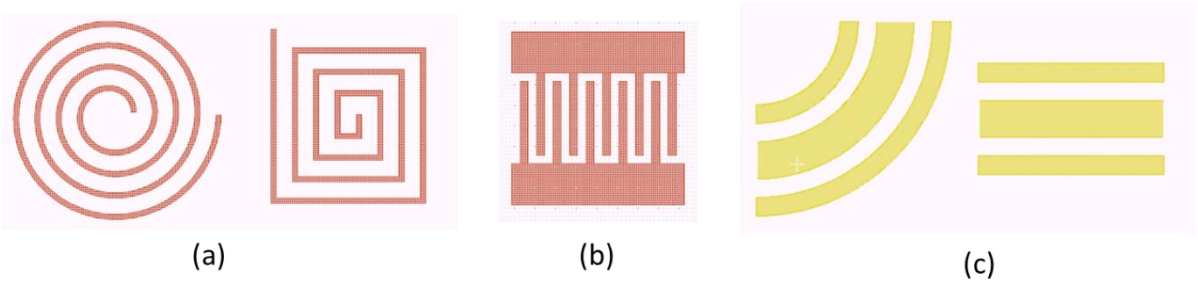

Figure 3: Examples of P-cells: a) Spiral and square inductors b) Finger capacitor c) CPW bend and straight waveguide.

3 Interconnecting devices with waveguides

The L-Edit PDK provided by CMC has a provision for automated CPW routing, in which the user can draw an "Orthogonal wire" by using the option [ ] in the toolbar and then convert this wire to a CPW routing P-cell. To create this cell, the user first selects the wire to be converted to CPW, and then goes to Tools → Photonics tools → Generate Auto Waveguide. This will convert the wire into a CPW routing, as illustrated in Fig. 4. Parameters such as width of central line and outer ground plane lines, spacing between lines and the radius of the bends can be modified in the "Edit Object" options in the toolbar [ ]. CPW routing can be used to make connections between various devices and to connect the components to the pads. It is a useful tool to draw layouts for superconducting circuits efficiently.

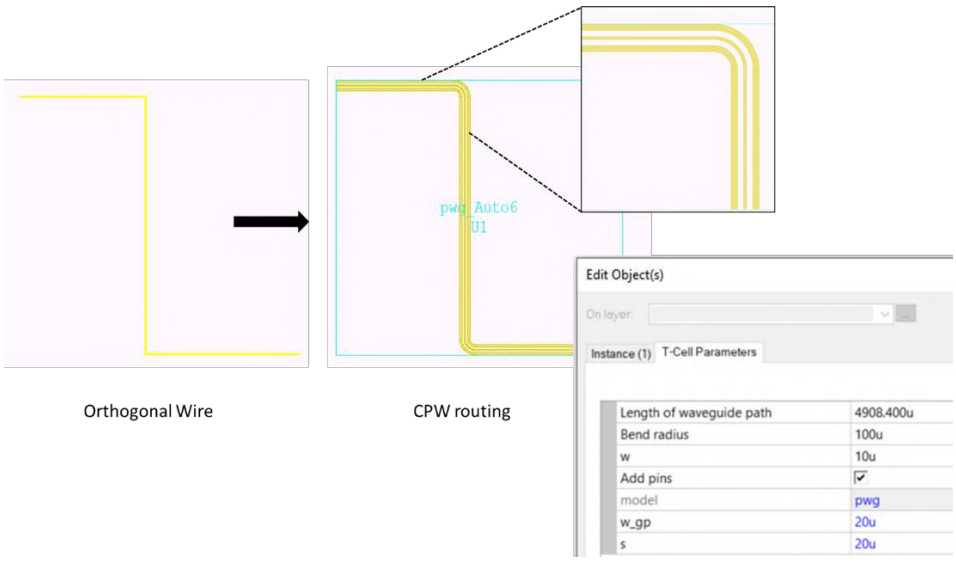

Figure 4: An orthogonal wire drawn is converted to a CPW routing. The parameters of the routing can be modified in the "Edit Object" window.

4 Superconducting quantum device design

In this section, we present an example of a typical superconducting quantum circuit designed with CMC library cells. Figure 5 shows two Josephson junctions, in a SQUID geometry, shunted by a finger capacitor which is connected to a feedline. The CPW P-cell is used to create the feedline and the ground planes, which are much wider than the central-line conductor. The ends of the CPW and the junctions are connected to the pads provided in the CMC library for the external connections. It is important to mention that the P-Cell parameters can be easily modified in the parameter window.

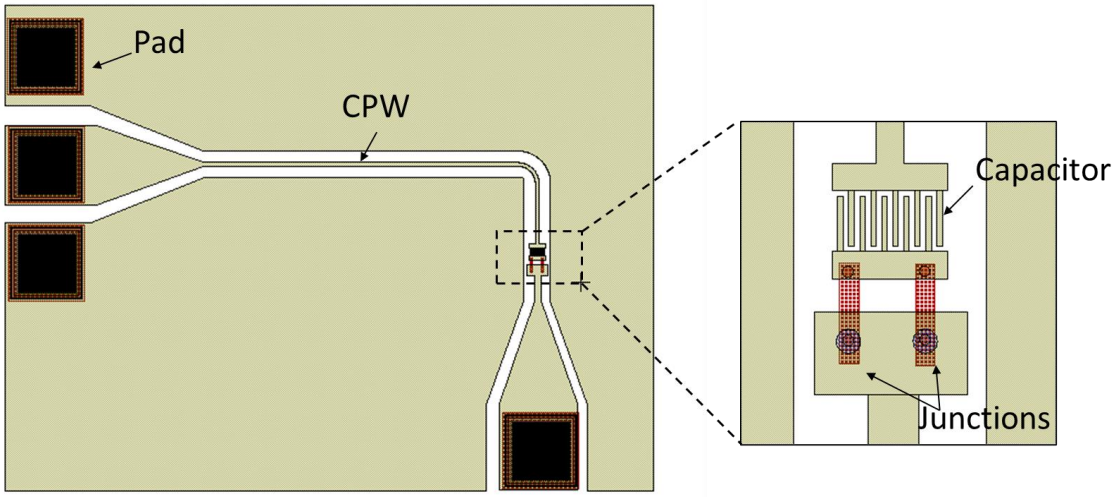

Figure 5: A quantum circuit designed using the CMC Cell Library and Siemens EDA's L-Edit.

Starting with P-cells and then interconnecting them in L-Edit, the superconducting quantum circuit can be easily designed and then verified using Calibre. After performing DRC, the design layout can be exported to an electromagnetic simulator to, for example, extract parameters that are used to model the quantum properties of the device.

Summary

In summary, we provided a brief description of the CMC PDK built for superconducting circuits on L-Edit. Various features of the L-Edit tool and PDK have been discussed to provide guidance for new users. The PDK will be updated regularly for CMC users participating in future superconducting multi-project wafer fabrication runs and CMC

Basecamp™ "Build Your Own Superconducting Quantum Device". For more information, please contact Quantum@cmc.ca.

References

[1] F. Arute et al., Quantum supremacy using a programmable superconducting processor, Nature volume **574**, 505 (2019).
[2] P. Jurcevic et al., Demonstration of quantum volume 64 on a superconducting quantum computing system**,** Quantum Sci. Technol. **6**, 025020 (2021).
[3] https://newsroom.ibm.com/2022-11-09-IBM-Unveils-400-Qubit-Plus-Quantum-Processor-and-Next-Generation-IBM-Quantum-System-Two
[4] L-Edit Photonics | Siemens EDA
[5] STAR Cryoelectronics | SQUID sensors, readout electronics, cryogenic systems & foundry services
[6] Tinkham, Michael, Introduction to Superconductivity 2nd edition, Dover Publications, 2004
[7] A. Blais, A. L. Grimsmo, S. M. Girvin, and A. Wallraff, Circuit quantum electrodynamics, Rev. Mod. Phys., 93, 025005 (2021).
[8] CAD Tools – CMC Microsystems