CORE-V™

OPENHW™

OpenHW Group

CORE-V: Open Source RISC-V Cores for Industry & Academia

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T @rickoco T @openhwgroup

www.openhwgroup.org

GROUP OPENHW® PROVEN PROCESSOR IP

- OpenHW Group is a not-for-profit, global organization registered in Canada and Europe. The OpenHW ecosystem is driven by members (corporate & academic) and individual contributors where HW and SW designers collaborate in developing open-source cores, related IP, tools and SW such as the CORE-V Family of open-source RISC-V processors
  - International footprint with developers in North America, Europe and Asia
  - Providing an infrastructure for hosting high quality open-source HW developments in line with industry best practices
  - Strong support from industry, academia and individual contributors worldwide

Industry Members

104+ Members & Partners

Academic Members

104+ Members & Partners

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

SIMON FRASER
UNIVERSITY

Universidade do Minho

Science and
Technology
Facilities Council

Partner Ecosystem

104+ Members & Partners

Accounting, Legal, Banking

Working Groups & Task Groups

- Board of Directors approves elected Chairs of Working Groups and has final approval of working group recommendations

- Technical Working Group
  - Cores Task Group
  - Verification Task Group
  - SW Task Group
  - HW Task Group
- Marketing Working Group
  - University Outreach Task Group

- OpenHW Asia Working Group
- OpenHW Europe Working Group

- Together with internal OpenHW Group engineering staff, member company development engineers (FTEs / ACs) establish and execute OpenHW Group projects
  - 20+ active projects across CORE-V RTL, Verification, GCC / LLVM, IDE, RTOS, FPGA, SoC, etc. with more projects in the pipeline

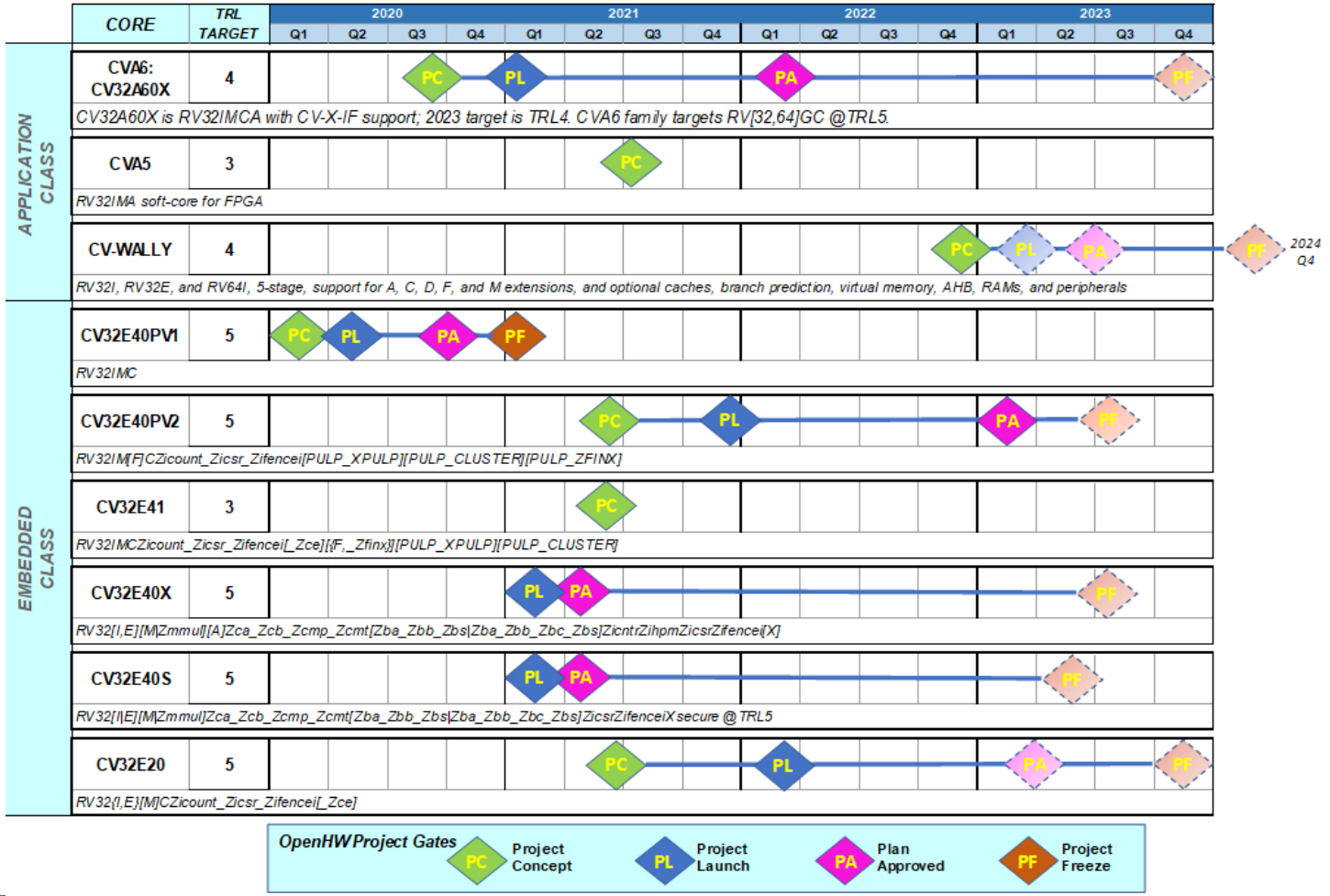
OpenHW Cores Task Group

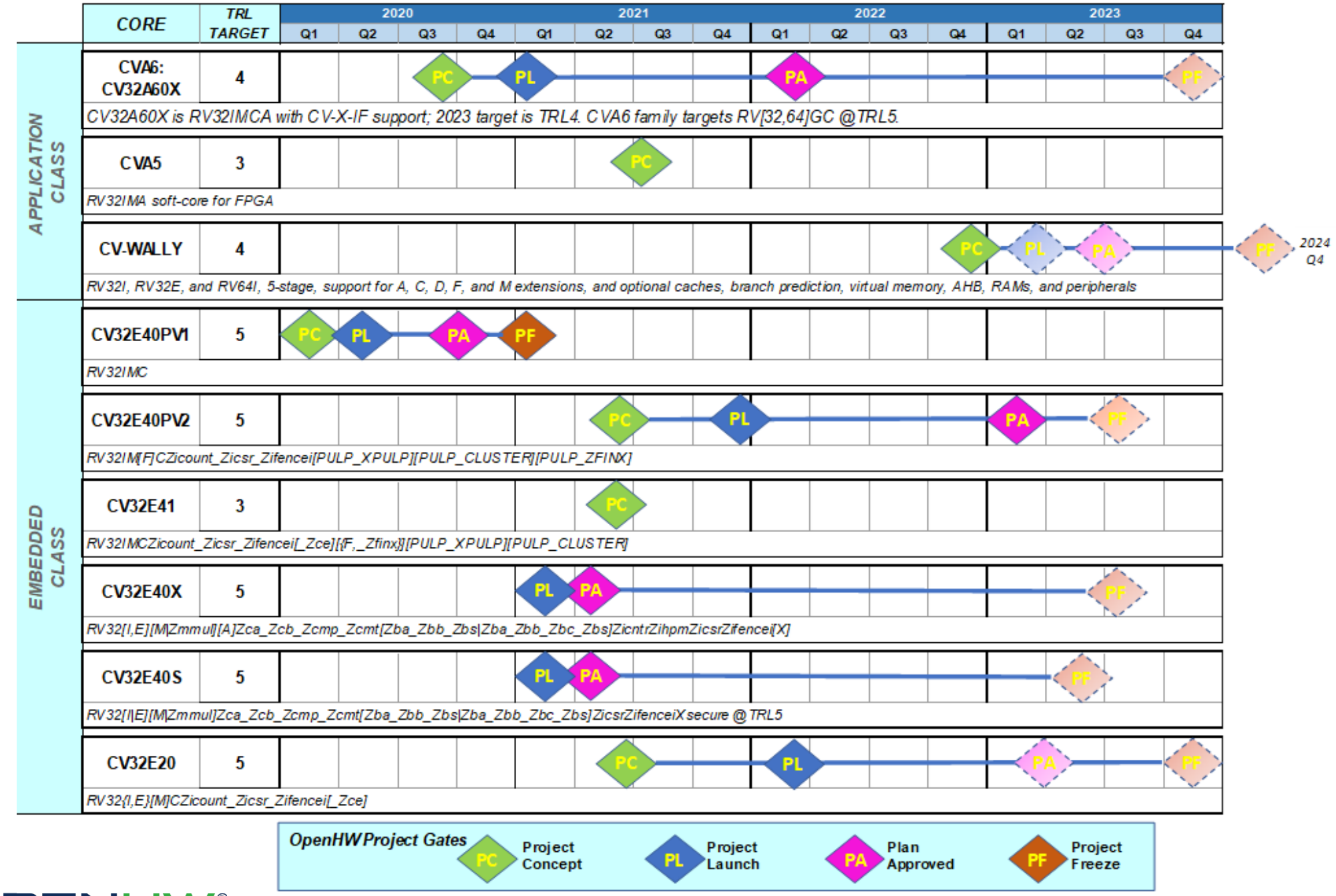
- Chair: Arjan Bink, Silicon Laboratories
- Vice-Chair: Jérôme Quévremont, Thales Research & Technology
- develop feature and functionality roadmap and the open-source IP for the cores within the OpenHW Group such as the CORE-V Family of open-source RISC-V processors.
- Initial contribution of open-source RISC-V cores from ETH Zurich PULP Platform and the OpenHW Group is the official committer for these repositories

Core	Bits/Stage	Description
CVE4 (RI5CY)	32bit / 4-stage	A family of 4-stage cores that implement, RV32IMFCXpulp, optional 32-bit FPU, instruction set extensions for DSP operations including HW loops, SIMD extensions, bit manipulation and post-increment instructions.
CVA6 (Ariane)	32 & 64bit / 6-stage	A family of 6-stage, single issue, in-order CPU cores implementing RV64GC extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. The cores have configurable size, separate TLBs, a HW PTW and branch-prediction (branch target buffer, branch history table and a return address stack).

CORE-V® Cores Roadmap

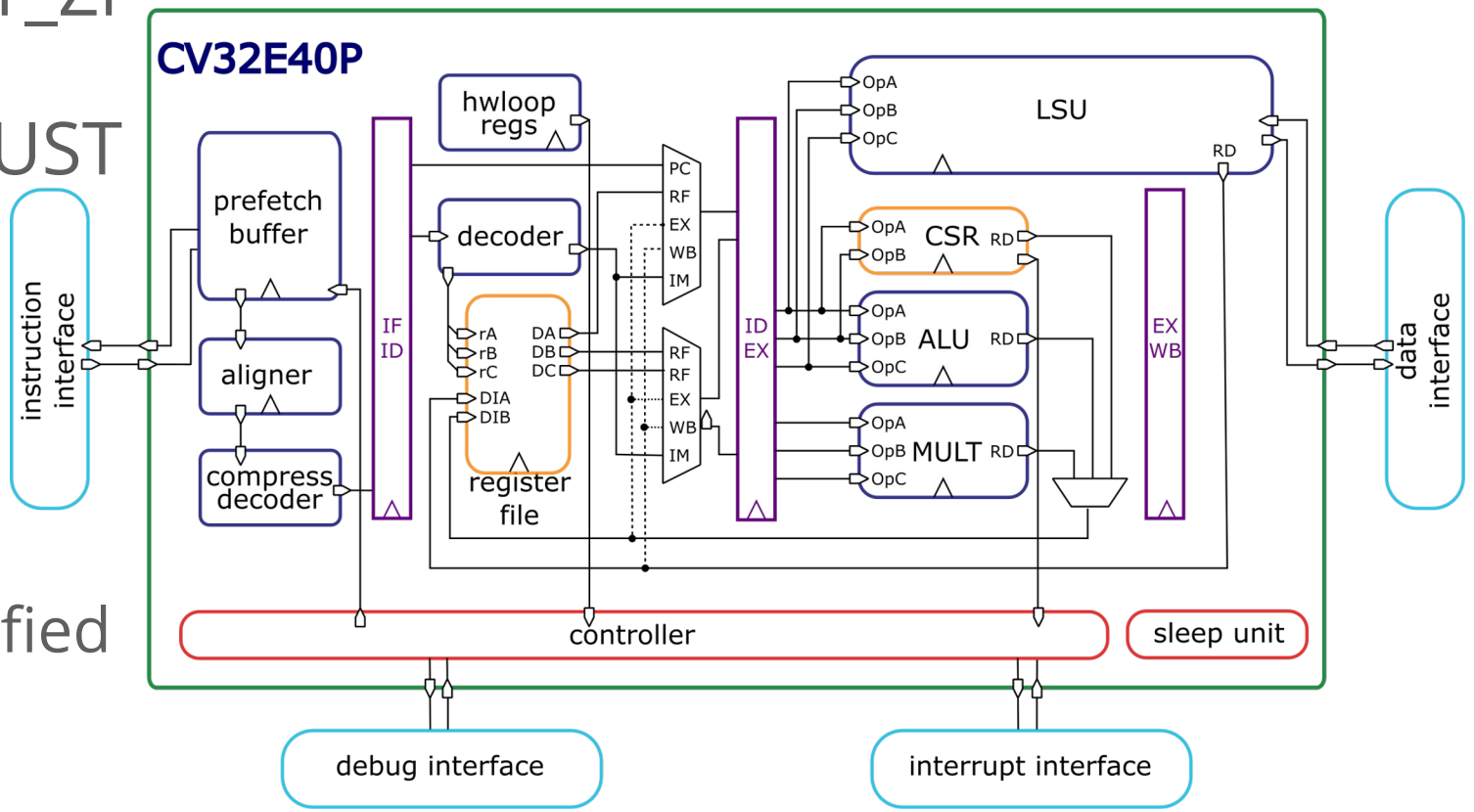
- OpenHW GitHub https://github.com/openhwgroup




CORE
TRL TARGET
2020
2021
2022
2023
Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4
APPLICATION CLASS
EMBEDDED CLASS
CVA6: CV32A60X
4
CV32A60X is RV32IMCA with CV-X-IF support; 2023 target is TRL4. CVA6 family targets RV[32,64]GC @TRL5.
CVA5
3
RV32IMA soft-core for FPGA
CV-WALLY
4
RV32I, RV32E, and RV64I, 5-stage, support for A, C, D, F, and M extensions, and optional caches, branch prediction, virtual memory, AHB, RAMs, and peripherals
2024 Q4
CV32E40PV1
5
RV32IMC
CV32E40PV2
5
RV32IM[F]CZicount_Zicsr_Zifencei[PULP_XPULP][PULP_CLUSTER][PULP_ZFINX]
CV32E41
3
RV32IMCZicount_Zicsr_Zifencei[_Zce][{F,_Zfinx}][PULP_XPULP][PULP_CLUSTER]
CV32E40X
5
RV32[I,E][M|Zmmul][A]Zca_Zcb_Zcmp_Zcmt[Zba_Zbb_Zbs|Zba_Zbb_Zbc_Zbs]ZicntrZihpmZicsrZifencei[X]
CV32E40S
5
RV32[I|E][M|Zmmul]Zca_Zcb_Zcmp_Zcmt[Zba_Zbb_Zbs|Zba_Zbb_Zbc_Zbs]ZicsrZifenceiXsecure @TRL5
CV32E20
5
RV32{I,E}[M]CZicount_Zicsr_Zifencei[_Zce]
PC
PL
PA
PF
OpenHW Project Gates
PC Project Concept
PL Project Launch
PA Plan Approved
PF Project Freeze

CVE4 Family CV32E40P

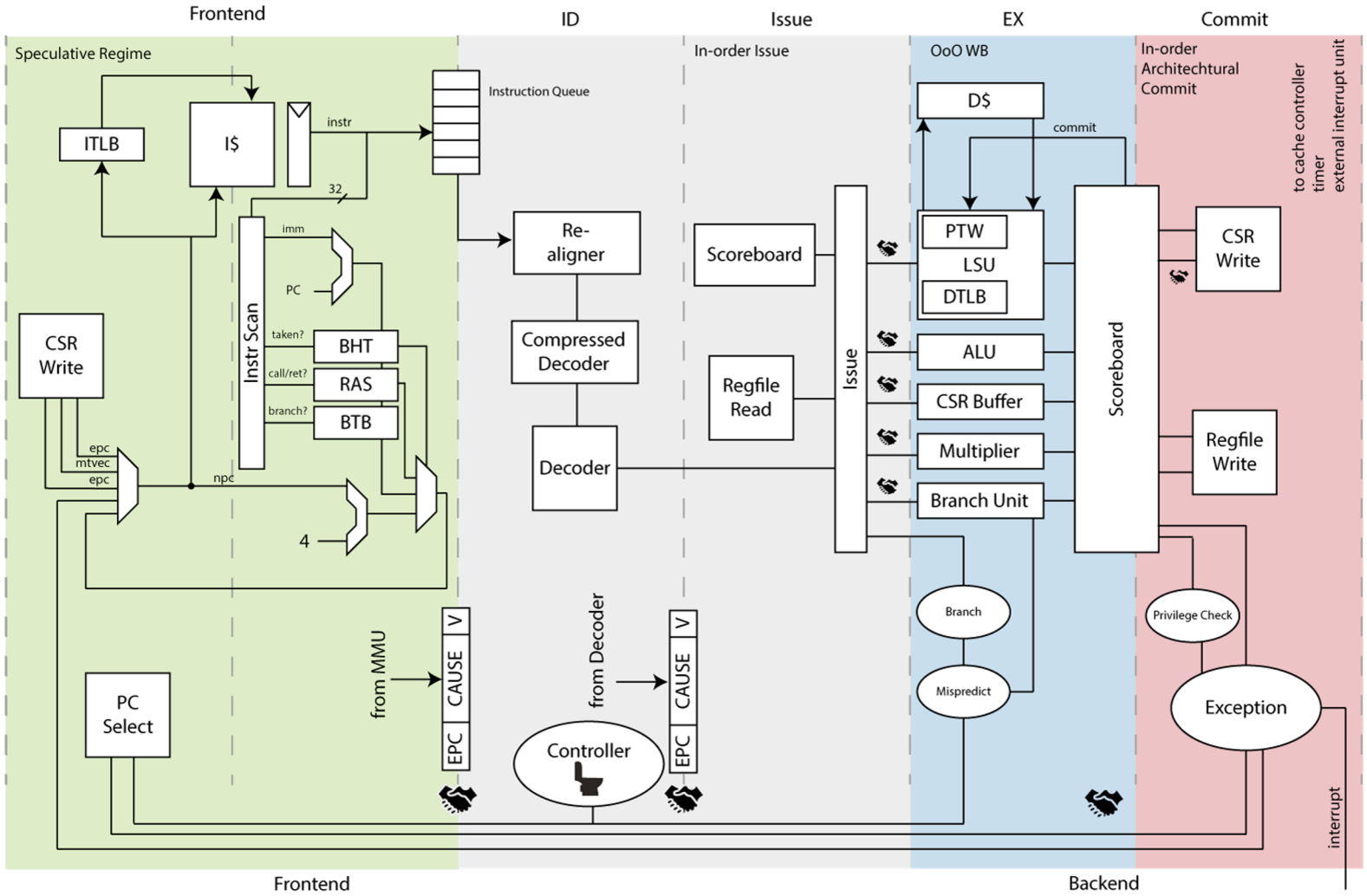
- 4-stage, in-order, single-issue
- RV32IM[F]CZicount_Zicsr_Zifencei [PULP_XPULP][PULP_CLUSTER][PULP_ZFINX]
- M-mode, CLINT, OBI
- ‘RTL Freeze’ achieved
  - RV32IMC extensions verified
  - Interrupts and Debug



CVA6 Family

- 6-stage, in-order, single-issue
- RV{32|64}IMAC[FD] Zicsr
- M/S/U-mode, CLINT, AXI

- Flexible application core
  - Linux-compatible thanks to MMU
  - 32 or 64 bit (CV32A6, CV64A6) from same RTL (64b from ETH, 32b from Thales)
  - L1 caches

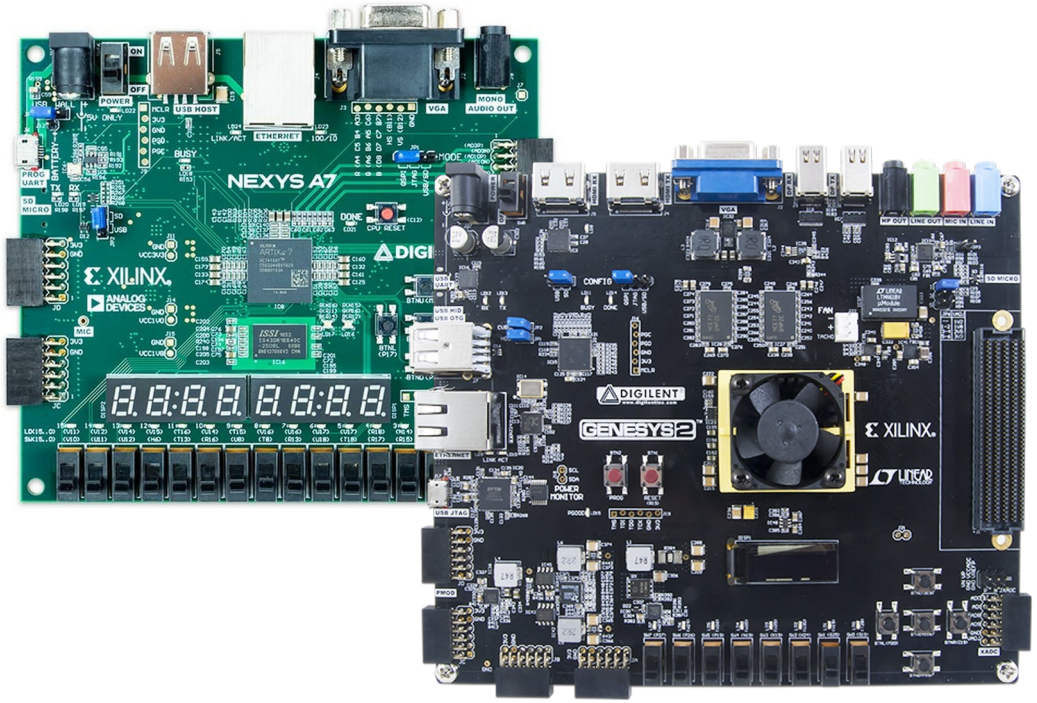


HW Task Group

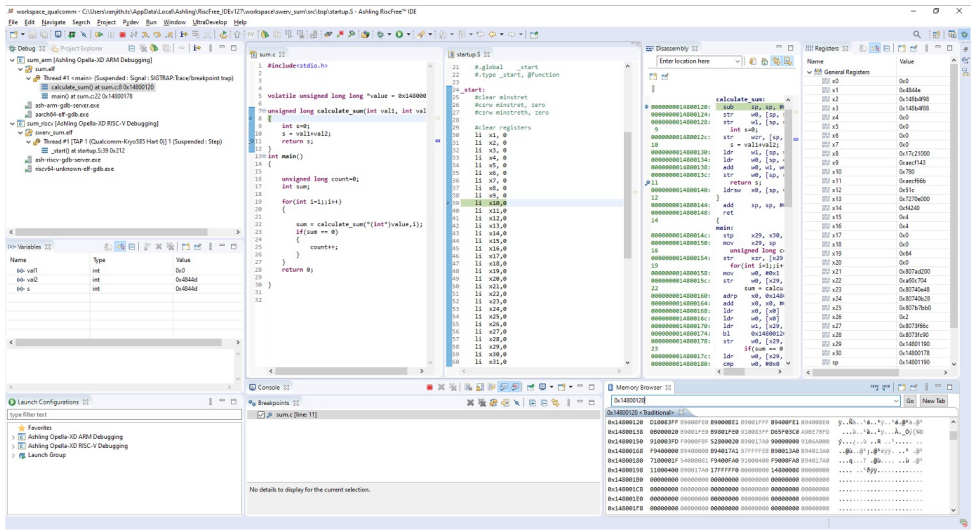
- Chair: Hugh Pollitt-Smith, CMC Microsystems
- Vice-Chair: Tim Saxe, QuickLogic
- define, develop and support SoC and FPGA based evaluation / development platforms for the cores and IP developed within the OpenHW Group.

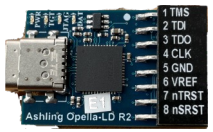
CORE-V® FPGA Emulation

- CORE-V projects leverage Digilent NexysA7 & Genesys2 FPGA boards for soft-core bring up for both CVE4 and CVA6 Families



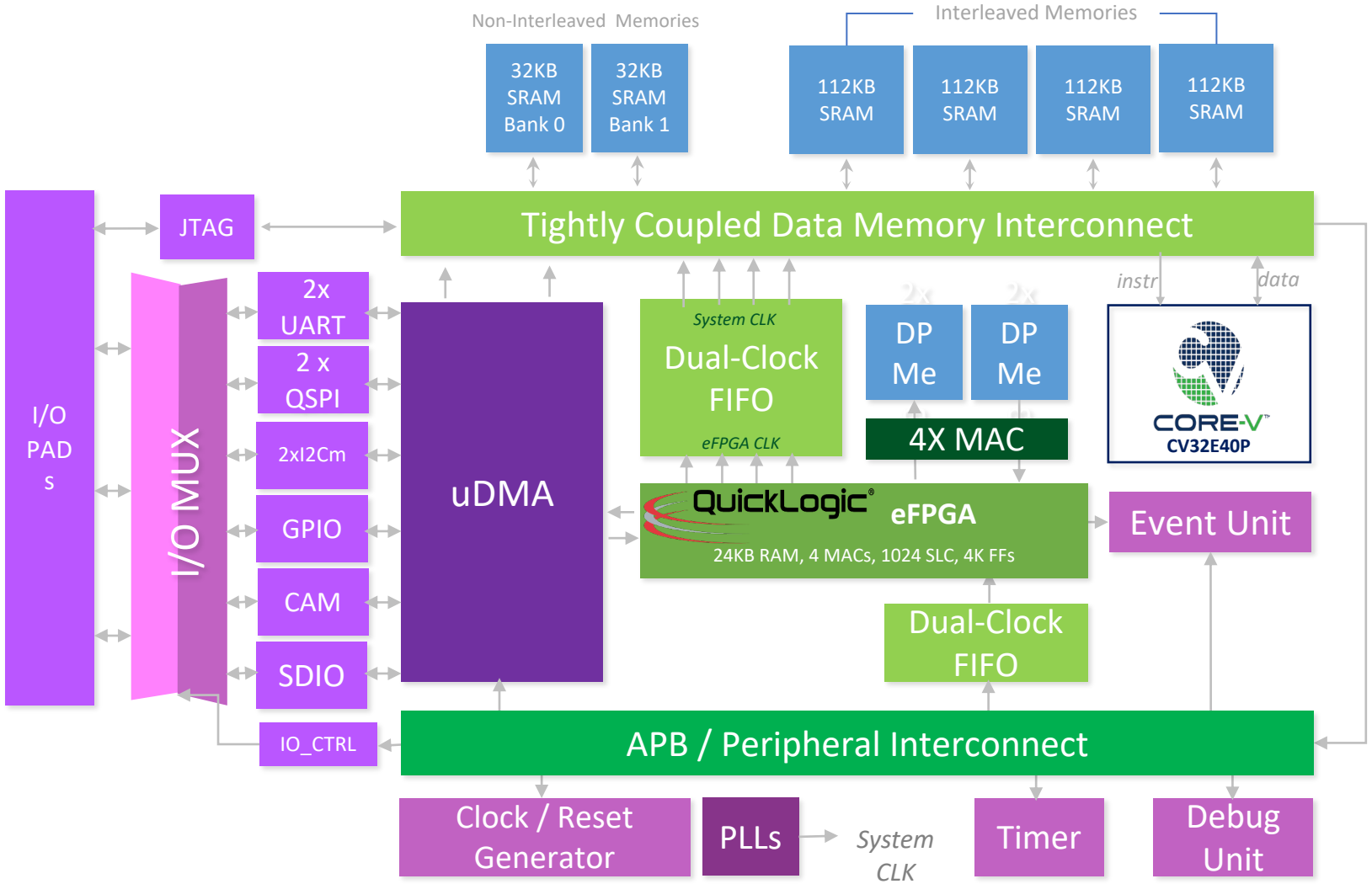
CORE-V™ IDE





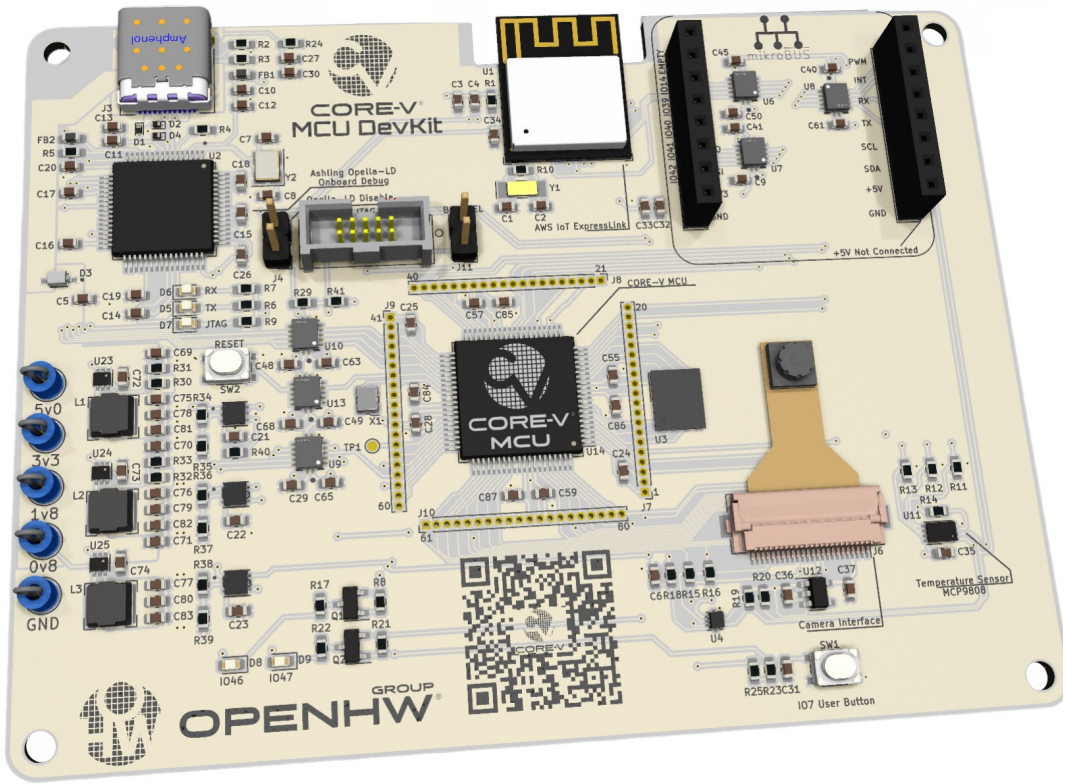
ASHLING Opella LD Debug Probe

CORE-V® MCU Tapeout 1st half 2023



- Real Time Operating System (e.g. FreeRTOS) capable ~300+MHz CV32E4 MCU
- Embedded FPGA fabric with hardware accelerators from QuickLogic
- Multiple low power peripheral interfaces (SPI, GPIO, I2C, HyperRAM, CAMIF, etc) for interfacing with sensors, displays, and connectivity modules
- Built in 22FDX with GF

CORE-V® MCU DevKit



OpenHW CORE-V DevKits

- CORE-V MCU SoC
  - CV32E40P processor core
  - Quicklogic ArticPro eFPGA
  - Global Foundries 22FDX
- Ashling Opella-LD onboard JTAG debug module
- USB-C for terminal and onboard debug access
- JTAG connector for external debug access
- Espressif AWS IoT ExpressLink Module for AWS IoT cloud interconnect
- mikroBUS onboard socket, allowing access to a vast range of mikroBUS modules
- 40 pin expansion header
- I2C temperature sensor
- Early Access CORE-V MCU DevKits can be reserved on the GroupGets campaign page (quantities are limited)

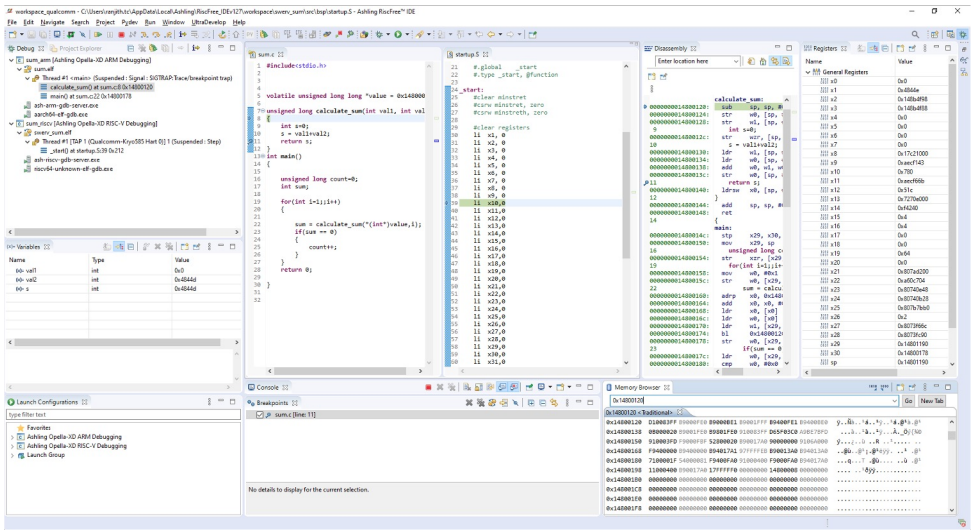
CVA6 - software support

- OpenSBI
- U-boot

- Linux
- FreeRTOS
- Yocto

- RISC-V standard toolchain (gcc, gdb, openOCD)

- Eclipse IDE

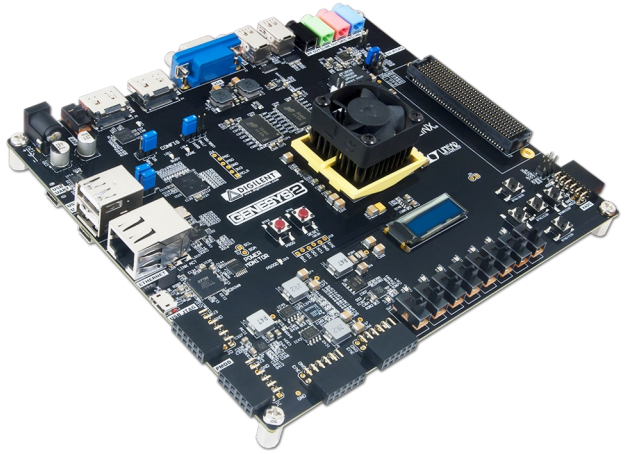


CVA6 – dual core SMP Linux on Genesys2

OpenPiton

CORE-V®

CVA6-SDK

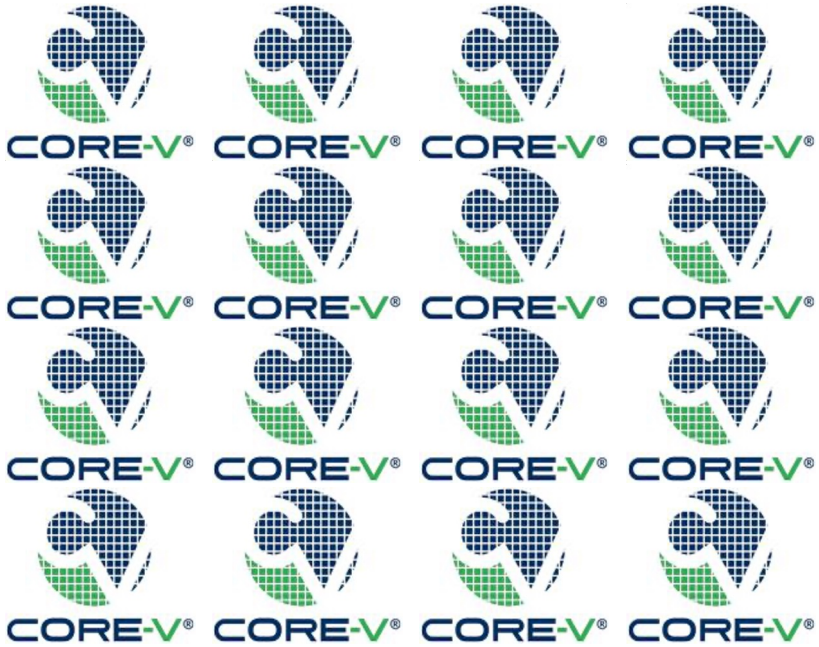


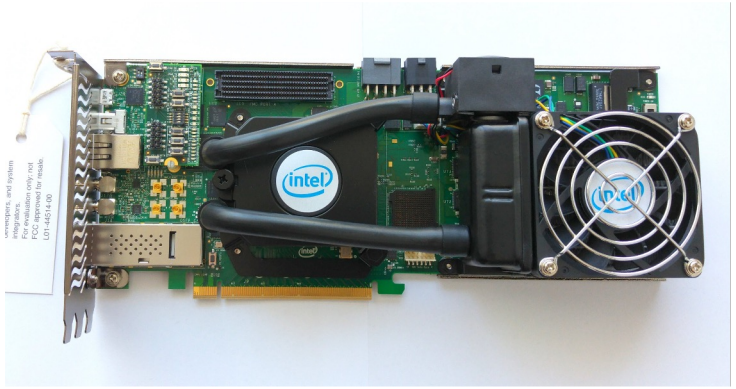
```
masgia@masgia-Inspiron-5579: ~
File  Edit  View  Search  Terminal  Help
[   12.580437] fff0c2c000.uart: ttyS0 at MMIO 0xfff0c2c000 (irq = 1, base_baud = 4166687) is a 16550
[   13.413954] printk: console [ttyS0] enabled
[   13.413954] printk: console [ttyS0] enabled
[   13.432853] piton_sd:v1.0 Apr 26, 2019
[   13.432853]
[   13.432853] piton_sd:v1.0 Apr 26, 2019
[   13.432853]
[   18.280307]  piton_sd: piton_sd1 piton_sd2
[   18.280307]  piton_sd: piton_sd1 piton_sd2
[   18.313435] libphy: Fixed MDIO Bus: probed
[   18.313435] libphy: Fixed MDIO Bus: probed
[   18.329267] xilinx_emaclite fff0d00000.ethernet: Device Tree Probing
[   18.329267] xilinx_emaclite fff0d00000.ethernet: Device Tree Probing
[   18.345813] libphy: Xilinx Emaclite MDIO: probed
[   18.345813] libphy: Xilinx Emaclite MDIO: probed
[   18.365367] xilinx_emaclite fff0d00000.ethernet: MAC address is now 00:18:3e:02:e3:e5
[   18.365367] xilinx_emaclite fff0d00000.ethernet: MAC address is now 00:18:3e:02:e3:e5
[   18.391571] xilinx_emaclite fff0d00000.ethernet: Xilinx EmacLite at 0x(____ptrval____) mapped to 0x(____ptrval____2
[   18.391571] xilinx_emaclite fff0d00000.ethernet: Xilinx EmacLite at 0x(____ptrval____) mapped to 0x(____ptrval____2
[   18.415544] ehci_hcd: USB 2.0 'Enhanced' Host Controller (EHCI) Driver
[   18.415544] ehci_hcd: USB 2.0 'Enhanced' Host Controller (EHCI) Driver
[   18.437508] usbcore: registered new interface driver usbhid
[   18.437508] usbcore: registered new interface driver usbhid
[   18.448971] usbhid: USB HID core driver
[   18.448971] usbhid: USB HID core driver
[   18.478182] NET: Registered protocol family 10
[   18.478182] NET: Registered protocol family 10
[   18.510941] Segment Routing with IPv6
[   18.510941] Segment Routing with IPv6
[   18.520527] sit: IPv6, IPv4 and MPLS over IPv4 tunneling driver
[   18.520527] sit: IPv6, IPv4 and MPLS over IPv4 tunneling driver
[   18.546628] NET: Registered protocol family 17
[   18.546628] NET: Registered protocol family 17
[   18.561907] Key type dns_resolver registered
[   18.561907] Key type dns_resolver registered
[   18.851667] Freeing unused kernel memory: 6724K
[   18.851667] Freeing unused kernel memory: 6724K
[   18.860994] This architecture does not have kernel memory protection.
[   18.860994] This architecture does not have kernel memory protection.
[   18.874036] Run /init as init process
[   18.874036] Run /init as init process
Starting logging: OK
Initializing random number generator... [   21.273658] random: dd: uninitialized urandom read (512 bytes read)
[   21.273658] random: dd: uninitialized urandom read (512 bytes read)
done.
Starting rpcbind: OK
[   22.539276] random: ssh-keygen: uninitialized urandom read (32 bytes read)
[   22.539276] random: ssh-keygen: uninitialized urandom read (32 bytes read)
Starting sshd: [   22.799293] random: sshd: uninitialized urandom read (32 bytes read)
[   22.799293] random: sshd: uninitialized urandom read (32 bytes read)
OK
NFS preparation skipped, OK

Welcome to Buildroot
buildroot login: root
#
CTRL-A Z for help | 115200 8N1 | NOR | Minicom 2.7.1 | VT102 | Offline | ttyUSB0
```

CVA6 – 16 core cluster on Stratix10

OPENHW®

OpenPiton





masgia@masgia-Inspiron-5579: ~

File Edit View Search Terminal Help

```
----------------------------------------
-- OpenHW CORE-V CVA6 P-Mesh Cluster  --
----------------------------------------
OpenPiton Version: b'5ee40e65'
CVA6 Version:    b'9275ad7a'

FPGA Board:        s10gx
Build Date:        Dec 12 2022 08:13:16

#X-Tiles:          4
#Y-Tiles:          4
#Cores:            16
Core Freq:         50 MHz
Network:           2dmesh_config
DRAM Size:         1024 MB

L1I Size / Assoc:   16 kB / 4
L1D Size / Assoc:    8 kB / 4
L15 Size / Assoc:    8 kB / 4
L2  Size / Assoc:   64 kB / 4
----------------------------------------


Hello from CVA6 ID 00
Hello from CVA6 ID 01
Hello from CVA6 ID 02
Hello from CVA6 ID 03
Hello from CVA6 ID 04
Hello from CVA6 ID 05
Hello from CVA6 ID 06
Hello from CVA6 ID 07
Hello from CVA6 ID 08
Hello from CVA6 ID 09
Hello from CVA6 ID 10
Hello from CVA6 ID 11
Hello from CVA6 ID 12
Hello from CVA6 ID 13
Hello from CVA6 ID 14
Hello from CVA6 ID 15
```

CTRL-A Z for help | 115200 8N1 | NOR | Minicom 2.7.1 | VT102 | Offline | ttyUSB0

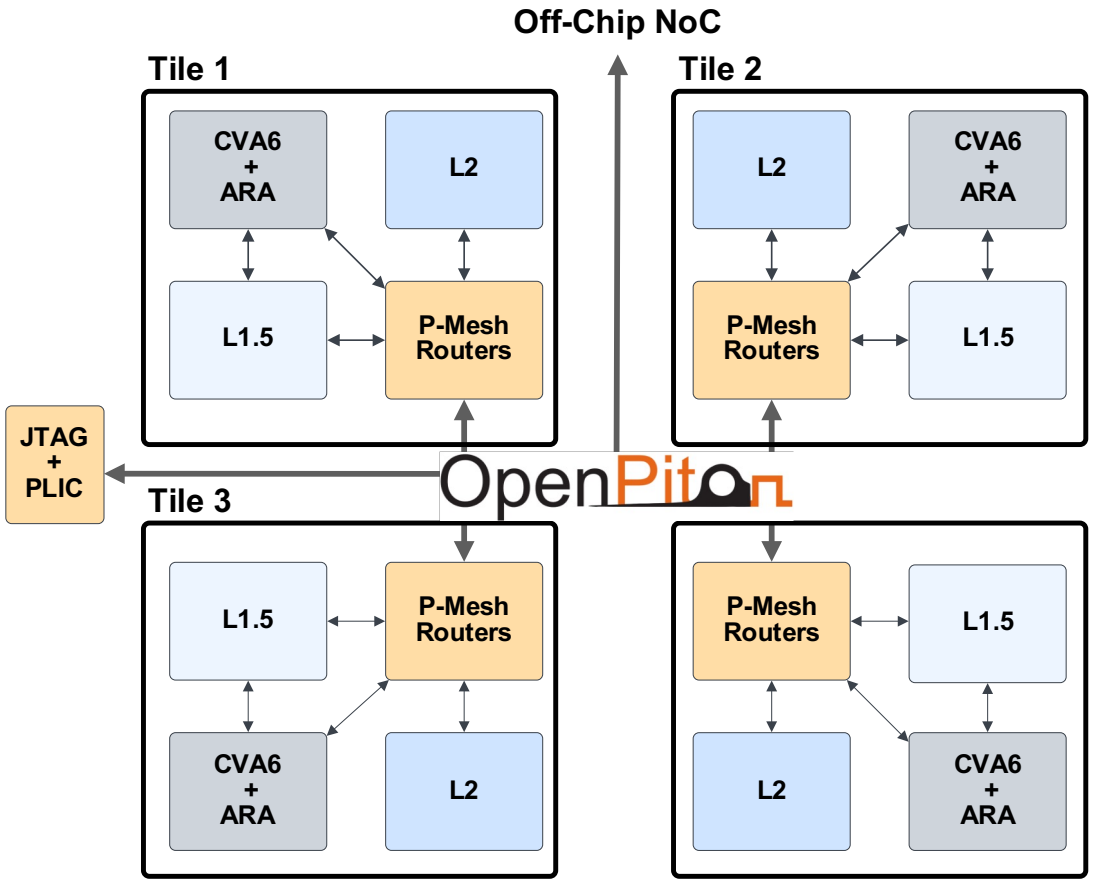
OpenHW Accelerate 1st Project

- 1st OpenHW Accelerate Co-Funded Project

  CORE-V CV-VEC: RISC-V Vector Processor for High-throughput Multidimensional Sensor Data Processing & Machine Learning Acceleration at the Edge

  - Gord Harling, Hugh Politt-Smith, CMC (Industry Sponsor)
  - Frank Gürkaynak, Matheus Cavalcante, Matteo Perotti, ETH Zürich
  - Yvon Savaria, Nizar El Zarif, Hossein Askari Hemmat, Yoan Fournier, Elisabeth Humblet, Polytechnique Montréal
  - Jonathan Balkind, Ci-Chian Lu, UC Santa Barbara

CORE-V Polara Quad core Architecture



- Adding latest CVVEC (Ara) with sub-byte computation support into OpenPiton.
- Adding latest CVA6 with accelerator interface support into OpenPiton.
- Developing OpenPiton to AXI interface to connect OpenPiton NOC to CVVEC.

CORE-V Polara ASIC design

Name	CORE-V Polara
Technology	GlobalFoundries 22FDX FD-SOI
Package	CPGA208
Target frequency[1]	$\geq$ 1 GHz
Power[2]	$\leq$ 1.25 W
Width	3 mm
Height	3 mm
Area	9 mm^2

	I/Os		
Type	Inputs	Outputs	Total
Power	112	0	112
VDDC	28	0	28
VDDIO	28	0	28
VSSC	28	0	28
VSSIO	28	0	28
Off-Chip Interface (OCI)	46	39	85
Reset	1	0	1
FLL & Clock	4	1	5
JTAG	4	1	5
Chip bridge (data)	37	37	74
Total	158	39	197

- CORE-V Polara **tape-out planned for this year**
  - **GF22FDX**
  - **3x3 mm die**
- Quad core SoC with **4** instances of **CVA6+CVVEC** at **4 lanes** each

- OpenHW Group & CORE-V Family of open-source RISC-V cores for use in high-volume production SoCs
  - Visit www.openhwgroup.org for community information
  - Visit OpenHW GitHub https://github.com/openhwgroup for projects
  - Learn more at OpenHW TV

- Follow us on Twitter @openhwgroup & LinkedIn OpenHW Group