UNTETHER A

Energy-Efficient AI Inference Acceleration with Untether AI

Untether AI Addresses Current and Future AI Pain Points

	A flexible, programmable	An architecture that scales	Extreme power efficiency	Support the right datatypes
Solution	日 (1) (1) (1) (1) (1) (1) (1) (1)			Ø
	Will evolve in unknown ways in the future	cloud to edge in the future	Forecast to be 15% due to the growth in inference deployments*	drift
	Neural net architectures are diverse today	Inference started in the cloud Will span from	1% of WW electricity usage is in the datacenter*	Deep quantization causes accuracy loss Analog techniques car
i Issue	Changing <mark>Al</mark> Workloads	Scalability	Efficiency and Performance	Accuracy

*source: Qualcomm

solution

runAI200[™] Device: Industry's First At-Memory Computation Engine

502 TOPs

- Optimized for INT8 inference
- 75W TDP, 50W typical

204MB on-chip SRAM

- 260 TB/s SRAM bandwidth
- Scalable voltage/frequency
- "Eco" and "Sport" modes, 8 TOPs/W
- 18.4B Transistors on TSMC 16nm
- 47.5 x 47.5 mm

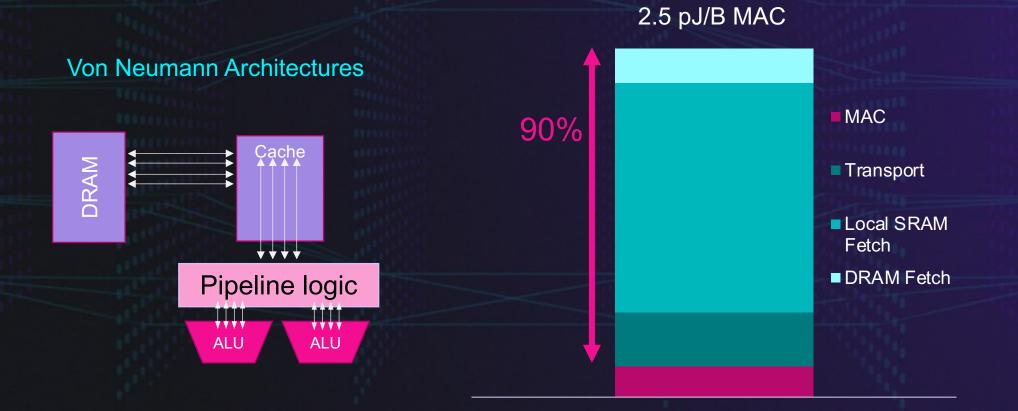
Al-tailored interconnect

• PCle Gen4 x16



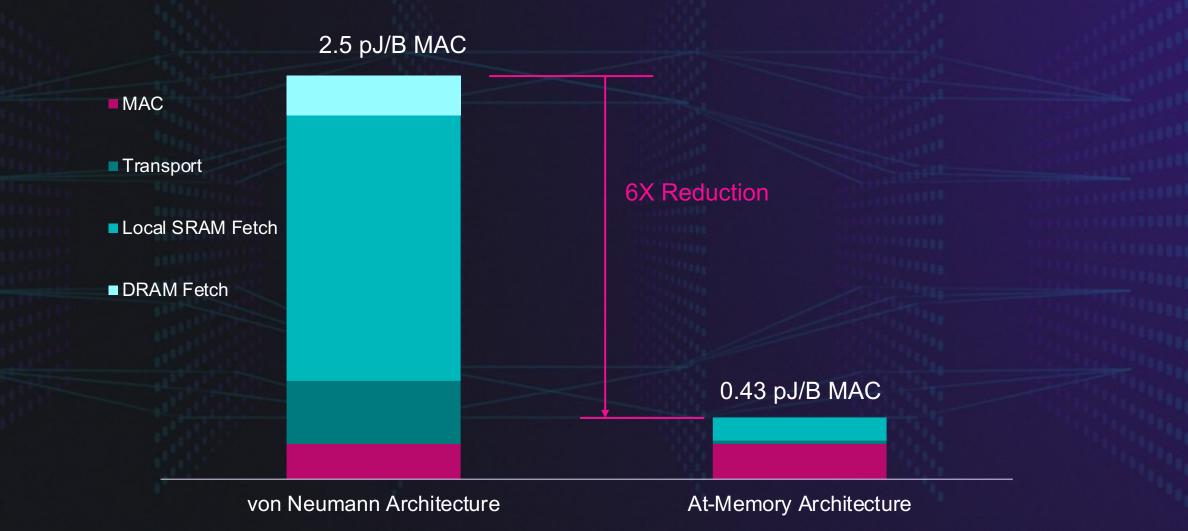
Von Neumann Approach is Wasteful

Data movement accounts for up to 90% of energy expended in a MAC operation



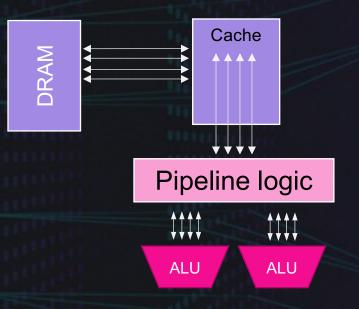
von Neumann Architecture

At-Memory Computing is 6x More Efficient



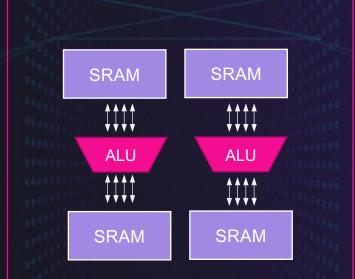
At-Memory Compute Is the Sweet Spot for AI Acceleration

Near Memory/ Von Neumann Architectures



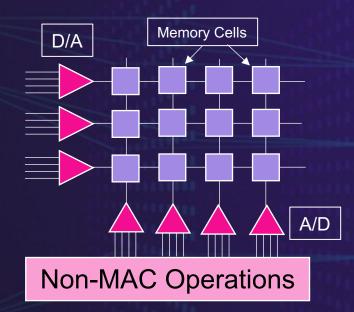
- Long, narrow busses
- Deep/shared cache





- Short, massively parallel direct connections
- Dedicated, optimized memory for efficiency and bandwidth

In-Memory Computation



- Multi-value memory cell
- Analog techniques used for multiplyaccumulate
- A/D and D/A support circuitry
- Digital processors for non-MAC operations

Innovative runAl Architecture

Direct Row Transfer

Column-based bank-to-bank local interconnect 32GB/s bank-to-bank 15TB/s total

X16 PCIe Gen4 Host connectivity 32GB/s

511 Memory Banks

512 Processing Elements

385K SRAM

RISC Controller

Rotator Cuff

Row-based bank-to-bank local interconnect

16GB/s bank-to-bank

8TB/s total

Pipelined Bus

Banks to PCIe connectivity Row-based ring 8GB/s per row 80GB/s Total

imAlgine Software Development Kit

Standard Frameworks and Formats

 TensorFlow, PyTorch, and ONNX supported

Robust Toolkit

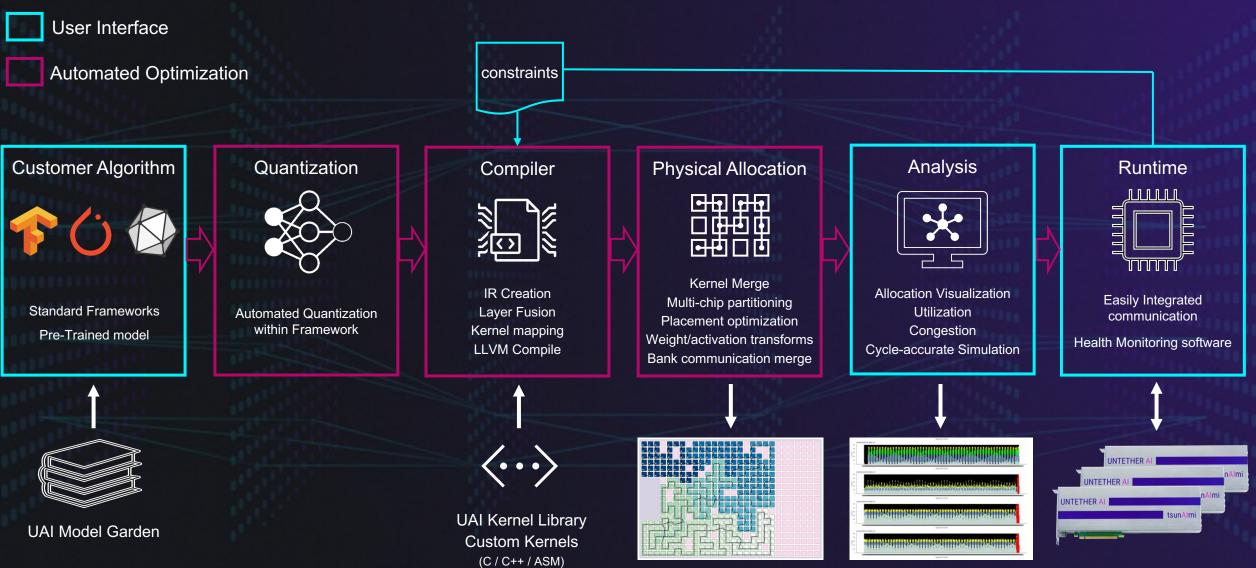
 All the right knobs exposed and tools available to go from trained models to inference ready models

Maintains Accuracy

• Quantizer retains as much accuracy as possible

Familiar frameworks Tensor	-low O PyTorc	
	a start at the sta	
imAlgine Compiler	imAlgine Toolkit	
Optmized graph lowering	Extensive allocation a simulation feedback	
im <mark>Al</mark> gine F	Runtime	
Easily integrated health monitoring	communication and g software	
	nAlmi	
	nAlmi	

imAlgine SDK Tool Flow



imAlgine SDK: Quantization

User Input



Automatic ML Framework Optimizations

Automated Quantization Advanced Quantization (AdaQuant) Optional Quantization Aware Retraining

TF Quantization Example

```
1 graph = U.read_pb("./resnet50_v1.pb")
2 model = UModel.from_graph_def(graph)
3
4 with U.calibrate(model, U.default_observer):
5 for images, _ in calibration_data:
6 model(images)
7
8 UQuant.quantize(model)
9 model.write_pb('rn50.pb')
```

10 !imaigine compile 'rn50.pb'

Output



imAlgine SDK: Compiler Optimization Options

or

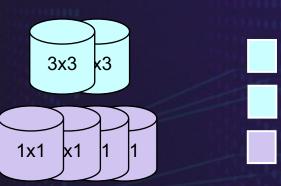
Optimize for Efficiency

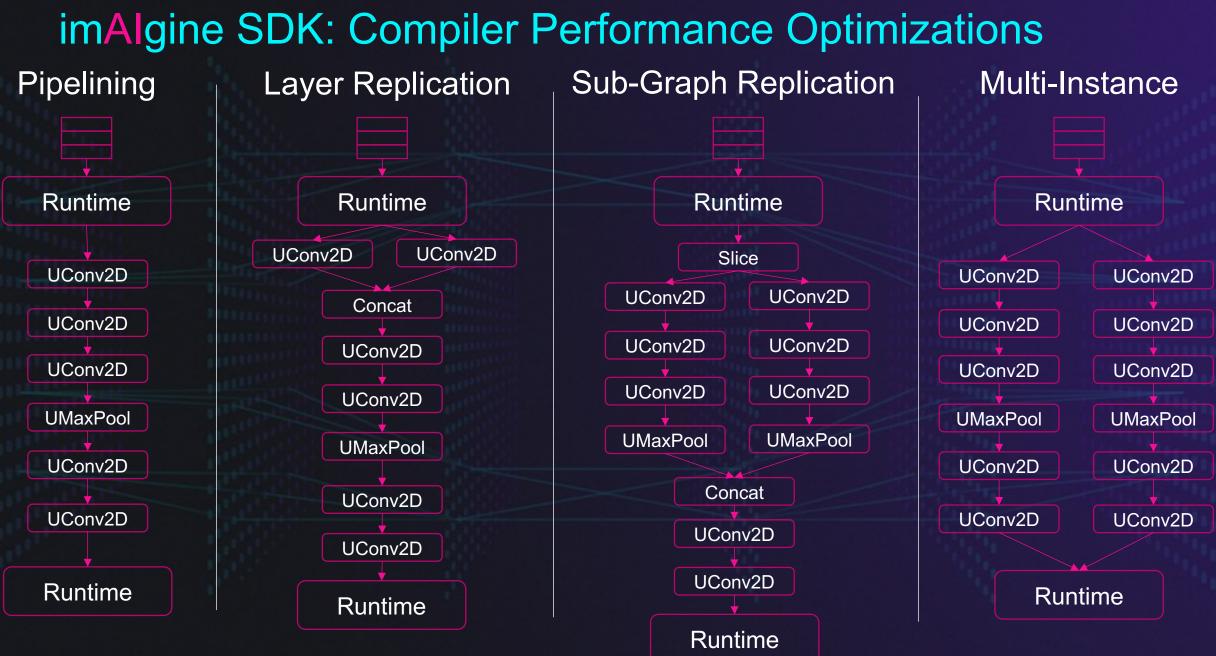
Fit in smallest area, least power



Optimize for **Performance**

Multiply instances to gain performance Unique for spatial architectures





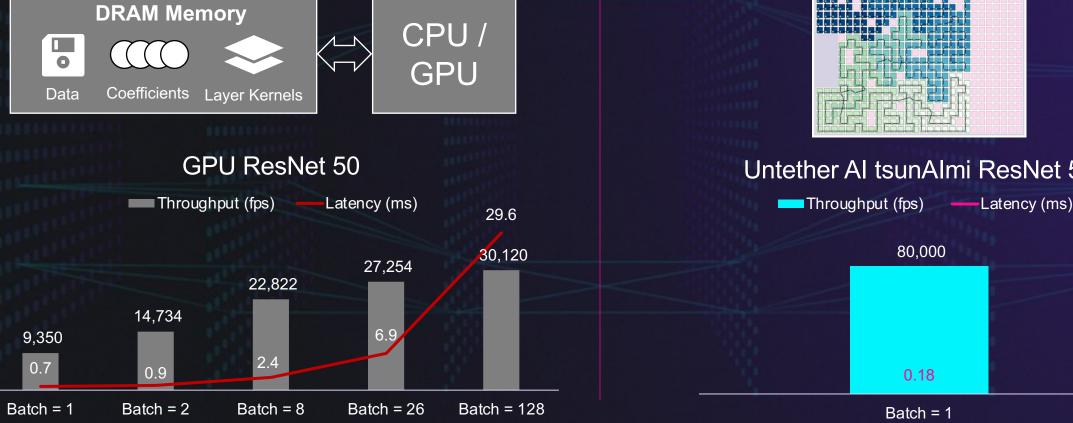
imAlgine SDK: Physical Allocation **CPU / GPU**

Needs to swap layers/coefficients from memory, batching data into larger groups helps with throughput, at the detriment of latency

Untether Al

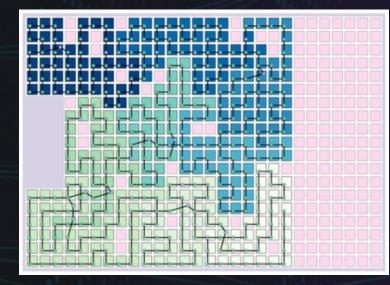
Places the entire network on chip, so is natively batch=1, providing

low latency and high throughput Untether AI tsunAlmi ResNet 50

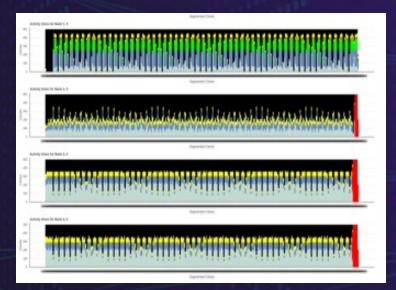


imAlgine SDK: Analysis & Cycle Accurate Simulation

Data Flow and Routing Visualization



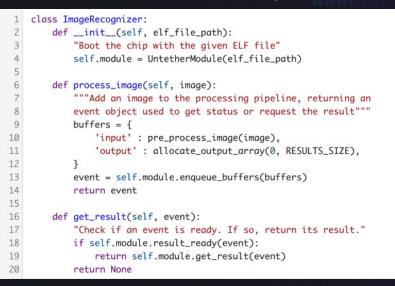
Simulation

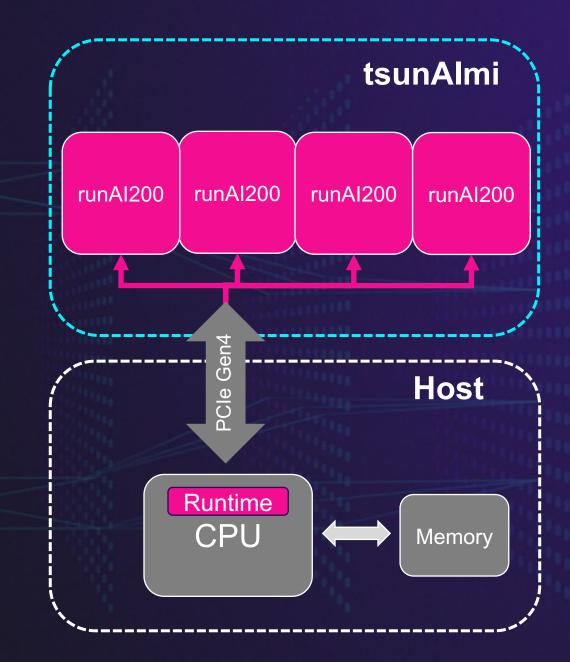


imAlgine SDK: Runtime

- High-Level API in ML framework
- Low-level API to access to various parts of the chip
- System management and debugging tools
- Health monitoring

Runtime API Example





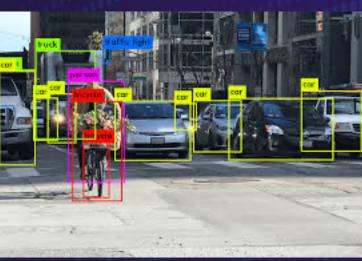
Next Step -> Getting Started

Version: 23.03-23.04

YOLOX-L Inference Demo

The YOLOX-L demo shows the performance of YOLOX-L running on the tsunAlmi card

untether-smi --set-profile=SPORT
make clean
make USE_COC0_DEM0=1
USE_COC0_DEM0=1 ./yolox1_demo -e <path_to_your_elf_file> -d <path_to_coco_dataset_dir>



Thank you